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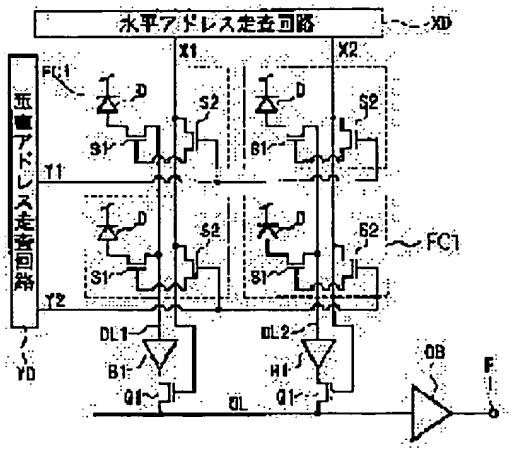
(54) IMAGE SENSOR



(57)Abstract:

PROBLEM TO BE SOLVED: To prevent a false signal such as smear and shading from being produced.

SOLUTION: A photodiode D is connected to a data line DL1 via a transistor(TR) S1 and connected to a horizontal address line X1 to connect a gate of a TR S2 controlling the TR S1 to a vertical address line. A data line is connected to a buffer B1 with a low input impedance and an output of the buffer is outputted to an output line OL via a TR Q1. When a vertical address line Y1 and the horizontal address line X1 are selected, a TR S2 is turned on and then the TR S1 is turned on the provide an output of charges stored in the photo diode D to the data line DL1 via the TR Q1. Since noise charges are given to the buffer B1 with a low input impedance, the charges are not stored in the data line and production of the false signal is suppressed.

CLAIMS

[Claim(s)]

[Claim 1] Image sensors equipped with two or more pixels which are characterized by providing the following and which are arranged at a plane, are chosen by the level address line and the perpendicular address line, and are connected to the data line. Each of the aforementioned pixel is a photo detector. Switching means which connect the aforementioned photo detector to the data line when both the level address line corresponding to the pixel concerned and the perpendicular address line are chosen. It connects between the aforementioned data line and an output line, and the aforementioned data-line side is the read-out means of a low input impedance.

[Claim 2] Image sensors according to claim 1 characterized by having the following, these 2nd switching means consisting of transistors, the gate of this transistor being connected to either the level address line or the perpendicular address line, and one side of electrodes other than the gate being connected to another side of the level address line or the perpendicular address line, and connecting the electrode of another side to the gate of the 1st switching means of the above. The 1st switching means by which the aforementioned switching means connect a photo detector to the data line alternatively. The 2nd switching means which turn ON the 1st switching means of the above when both the level address line and the perpendicular address line are chosen.

[Claim 3] Image sensors according to claim 2 characterized by attaching a charge electric discharge means to discharge the charge which remains in the 1st switching means at the 1st switching means of the above, at the time of un-choosing [of the level address line and the perpendicular address line].

[Claim 4] Image sensors according to claim 3 characterized by the resistance whose aforementioned charge electric discharge means connects the aforementioned gate of the 1st switching means to fixed potential while the aforementioned photo detector is a photodiode, the 1st switching means of the above consist of transistors, the gate of this transistor is connected with the 2nd switching means of the above, one side of electrodes other than the gate is connected to the aforementioned photodiode and the electrode of another side is connected to the aforementioned data line, or a current source to the bird clapper.

[Claim 5] Image sensors equipped with two or more pixels which are characterized by providing the following and which are arranged at a plane, are chosen by the level address line and the perpendicular address line, and are connected to the data line. The photo detector of the aforementioned pixel which consists of a photodiode, respectively. The 1st transistor which connects the anode of this photodiode to the data line. While having the 2nd transistor which connects a cathode to fixed potential and connecting the gate of the 1st transistor of the above to either the level address line or the perpendicular address line, the gate of the 2nd transistor is connected to another side of the level address line and the perpendicular address line, and the aforementioned data line is a low input impedance.

[Claim 6] Image sensors according to claim 1, 2, 3, 4, or 5 characterized by the aforementioned read-out means consisting of the buffer or amplifier which has a low input impedance, and the output selection means or the addition means of connecting the output and output line of the aforementioned buffer or amplifier when the aforementioned photo detector is connected to the data line linked to the read-out means concerned.

[Claim 7] Image sensors according to claim 1, 2, 3, 4, or 5 characterized by for the aforementioned read-out means having the buffer or amplifier which has a low input impedance and a high power impedance, and carrying out the direct file of the output of this buffer or amplifier to the aforementioned output line.

[Claim 8] Image sensors according to claim 7 characterized by equipping the aforementioned buffer or amplifier with a grounded-source type transistor circuit.

[Claim 9] Image sensors according to claim 7 characterized by equipping the aforementioned buffer or amplifier with current Miller circuit.

[Claim 10] Image sensors according to claim 7 characterized by equipping the aforementioned buffer or amplifier with a grounded-gate type transistor circuit.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] This invention relates to the image sensors which used the photo detector.

[0002]

[Description of the Prior Art] As conventional image sensors, there is a thing as shown in drawing 12 ; for example. Two or more pixel FC5a which consists of transistors S11 MOS type [for a switch] which connect alternatively to the data line the photodiode D these image sensors of whose are photo detectors, and a photodiode, FC5b, FC5c, and FC5d are arranged in the shape of two-dimensional.

[0003] Pixel FC5a corresponding to the level address line X1 and the perpendicular address line Y1 is taken for an example, and the composition is explained. Photodiode D is connected to the data line DL1 through the transistor S11. The gate of a transistor S11 is connected to the perpendicular address line Y1. The data line DL1 is connected to the output line OL through the transistor Q4 MOS type [for a switch] which connects this data line DL1 to an output line OL alternatively. The output line OL is connected to the output terminal P through output-buffer alumnus. The gate of a transistor Q4 is connected to the level address line X1. The perpendicular address line Y1 and the level address line X1 are connected to the perpendicular address scanning circuit YD and the level address scanning circuit XD which consist of a shift register, respectively.

[0004] In these image sensors, the charge by which photo electric translation was carried out to the period when the transistor S11 is turned off according to the amount of incident lights is accumulated at Photodiode D. First, if the level address line X1 is chosen as the degree by which the charge accumulated by turning on [it] a transistor S11 at Photodiode D will be distributed to the data line DL1 if the perpendicular address line Y1 is chosen, a transistor Q4 will be turned on [it], the data line DL1 is connected with an output line OL, and the charge of the data line DL1 is sent to output-buffer alumnus through an output line OL. Thereby, the charge stored in Photodiode D can be read.

[0005]

[Problem(s) to be Solved by the Invention] However, there was a problem that aliases, such as a smear

and shading, occurred, in such conventional image sensors. First, a smear is explained. As for the photodiode of the line connected to the perpendicular address line, all are connected to each data line while the perpendicular address line is chosen. For example, the charge stored in the photodiode D of pixel FC5c is also distributed to the data line DL2 at the same time the charge stored in the photodiode D of pixel FC5a will be distributed to the data line DL1, if the perpendicular address line Y1 is chosen in order to read the charge of the photodiode D of pixel FC5a. On the other hand, since the transistor Q4 which connects the data line DL2 and an output line OL turns off, the data line DL2 is in the high impedance state. Therefore, the distributed charge will be stored in the data line DL2, and the potential of the data line DL2 will rise.

[0006] If the quantity of light which carried out incidence to the photodiode D of pixel FC5c is large, since there are also many the charges, the potential of the data line DL2 becomes high, the threshold of the transistor S11 of other pixel FC5d linked to the data line DL2 is exceeded, it will become impossible to maintain an OFF state, the charge in the data line DL2 will leak to the photodiode D of pixel FC5d through a transistor S11, and the transistor S11 will be accumulated.

[0007] This phenomenon is called saturation of the data line and causes a smear. It becomes the picture which the smear SU as if a light strong against all the pixels of the train carried out [if the data line was not saturated,] incidence as shown in (b) of drawing 13 when a picture as shown in (a) of drawing 13 was acquired, and the data line of the train of the light source H was saturated generated. In addition, the smear is the same, even if an MOS transistor also generates P type or N type and the photodiode is operating in solar-battery mode. Although using it, lowering the dynamic range is performed in order to prevent generating of a smear, if it does so, since a range is insufficient, sufficient picture will no longer be acquired at the time of photography or photography of night.

[0008] Next, shading is explained. When there is no incident light in all the photodiodes D when using image sensors in the pitch-black state, and read-out is performed, shading may occur. The perpendicular address line Y1 is chosen first, and, next, read-out is chosen in order of the level address lines X1 and X2. In case the transistor S11 of pixel FC5a and the transistor Q4 connected to the data line DL1 turn on, a charge is supplied from the exterior, a part of supplied charge passes along the parasitic capacitance between the gate and a substrate, and it leaks to a substrate. The charge which leaked to the substrate is injected into the source and the drain of a transistor S11 in pixel FC5c or pixel FC5d by capacity coupling and diffusion.

[0009] Since the transistor Q4 connected to the data line DL2 at this time turns off, the data line DL2 is in the high impedance state, and the leaked charge is stored in the data line DL2 linked to the source of S11. Next, if the data line DL2 is chosen, the transistor Q4 connected to DL2 will be turned on [it], and the stored leakage charge will be read as an alias. Since the leakage charge is added as the scan of the address line progresses, the picture turns into a picture which the luminosity increases by the scanning direction of **** as shown in (c) of drawing 13 .

[0010] Furthermore, in case these image sensors are used for an image processing, they have the problem that random access cannot be done. That is, in case an image processing is performed, the random access function which reads arbitrary pixels in arbitrary turn is required. However, in these conventional image sensors, read-out is divided into two stages, and is performed, perpendicular address-line Y is chosen first, and the charge stored in the photodiode D of the line is distributed to the data line DL connected, respectively. Next, level address-line X is chosen and each charge of DL is read to an output line OL.

[0011] For example, when reading the charge of the photodiode D of FC5a, the charge of the photodiode D of FC5c will also be distributed to the data line DL2. Next, first, if it is going to read the charge of the photodiode D of FC5d, in order to throw away the charge of the data line DL2, dummy

read-out must be performed once and the data line DL2 must be reset. If the photodiode D of FC5d is read, the charge of the photodiode D of FC5c will be thrown away and, next, the charge of the photodiode D of FC5c cannot be read.

[0012] Therefore, this invention aims at being able to prevent generating of aliases, such as a smear and shading, and offering the image sensors in which random access is possible in view of the above-mentioned conventional trouble.

[0013]

[Means for Solving the Problem] For this reason, this invention according to claim 1 is arranged at a plane, is chosen by the level address line and the perpendicular address line, and is set to image sensors equipped with two or more pixels connected to the data line. It has the switching means which connect a photo detector to the data line when both the level address line corresponding to a photo detector and the pixel concerned in each of a pixel and the perpendicular address line are chosen. The data line shall be connected to an output line through a read-out means to have a low input impedance.

[0014] The 1st switching means by which the above-mentioned switching means connect a photo detector to the data line alternatively, It consists of the 2nd switching means which turn ON the 1st switching means when both the level address line and the perpendicular address line are chosen. The 2nd switching means consist of transistors and the gate of a transistor is connected to either the level address line or the perpendicular address line. One side of electrodes other than the gate shall be connected to another side of the level address line or the perpendicular address line, and the electrode of another side shall be connected to the 1st switching means.

[0015] It is desirable to attach further a charge electric discharge means to discharge the charge which remains in the 1st switching means at the time of un-choosing [of the level address line and the perpendicular address line] to the 1st switching means. Moreover, the above-mentioned photo detector is made into a photodiode, the 1st switching means are constituted from a transistor, and while connecting the gate of this transistor with the 2nd switching means, connecting one side of electrodes other than the gate to a photodiode and connecting the electrode of another side to the data line, a charge electric discharge means can constitute the gate of the 1st switching means from the resistance or the current source linked to fixed potential.

[0016] A pixel invention according to claim 5, respectively Moreover, the photodiode as a photo detector, The 1st transistor which connects the anode of this photodiode to the data line, While having the 2nd transistor which connects a cathode to fixed potential and connecting the gate of the 1st transistor to either the level address line or the perpendicular address line The gate of the 2nd transistor shall be connected to another side of the level address line and the perpendicular address line, and the data line shall be connected to an output line through a read-out means to have a low input impedance.

[0017] In each invention, the above-mentioned read-out means can consist of the buffer or amplifier which has a low input impedance, and an output selection means to allow the output of a buffer or amplifier, and connection of an output line only when a photo detector is connected to the data line linked to the read-out means concerned.

[0018] Or a read-out means shall have the buffer or amplifier which has a low input impedance and a high power impedance, and shall carry out the direct file of the output of the buffer or amplifier to an output line again. Under the present circumstances, the buffer or amplifier of a low input impedance and a high power impedance shall be equipped with grounded-source type a transistor circuit, current Miller circuit, or a grounded-gate type transistor circuit.

[0019]

[Function] In the thing of a claim 1, in each pixel, switching means connect the photo detector of the

pixel concerned to the data line, when both the level address line and the perpendicular address line are chosen. That is, since a transistor S12 is arranged as switching means which connect a photo detector and the data lines, such as Photodiode D, and these switching means are controlled by the compound address (xi-yj) (i= 1, 2, ..., j= 1, 2, ...) of the perpendicular address and the level address to be shown in drawing 14 , each pixel can be read independently and random access becomes possible.

[0020] By the way, if the direct file of the data line and the output line is carried out, the new problem that the parasitic capacitance of an output line increases will arise. That is, if all the data lines are connected to an output line, the parasitic capacitance of the switch in all pixels will work as a parasitic capacitance of an output line, the parasitic capacitance of an output line will become large, and a speed of response will become slow. For example, when there are the 512x512 numbers of pixels, the parasitic capacitance of the switch for 512x512 pieces is connected to the data line. In the conventional example, since the switch linked to an output line is 512x2 pieces, the parasitic capacitance of an output line becomes a bird clapper to (512x512) / (512x2) =256 time of the parasitic capacitance of the conventional example.

[0021] In this invention, since the data line is connected to the output line through a read-out means to have a low input impedance, a bird clapper is prevented for the data line by high impedance, and the parasitic capacitance of an output line does not increase. Since a bird clapper does not have the data line in high impedance, a smear and shading are also prevented.

[0022] In addition, it is simply constituted using a transistor, respectively by dividing switching means into the 1st switching means and 2nd switching means. Moreover, by attaching the charge electric discharge means of connecting the gate of the transistor to fixed potential by resistance etc. to the 1st switching means which connect a photo detector to the data line alternatively, at the time of un-choosing [of the level address line and the perpendicular address line], the charge which remains in the 1st switching means discharges, and it is not concerned in order of the non-choosing change of the level address line and the perpendicular address line, but is intercepted certainly.

[0023] Moreover, when a read-out means shall have the buffer or amplifier which has a low input impedance and a high power impedance, even if it carries out the direct file of the output of the buffer or amplifier to an output line, the output of other pixels does not flow backwards from an output-line side.

[0024] In the thing of a claim 5, since the two poles of the photodiode as a photo detector of each pixel are connected to the 1st transistor and 2nd transistor and it is not necessary to connect with fixed potential, constituting on an insulating substrate is easy.

[0025]

[Embodiments of the Invention] An example explains the gestalt of implementation of invention. Drawing 1 is drawing showing the 1st example of this invention. The n level address lines X1-Xn connected to the m perpendicular address lines Y1-Ym by which these image sensors were connected to the perpendicular address scanning circuit YD, and the level address scanning circuit XD are arranged in the shape of a grid, and the n data lines DL1-DLn are arranged together with the level address lines X1-Xn. A pixel FC1 consists of MOS type transistors S2 connected at MOS type the transistor S1 and the perpendicular address line for the switch which connects to the data line alternatively the photodiode D which is a photo detector, and a photodiode.

[0026] The pixel FC1 of an mxn individual is arranged in the shape of two-dimensional, and each pixel FC1 is controlled by the perpendicular address y on the perpendicular address line, and the level address x on the level address line. In order to simplify explanation, the image sensors in m= 2 and n= 2 are shown in drawing 1 . The pixel FC1 connected to the perpendicular address line Y1 and the level address line X1 is taken for an example, and the composition is explained. The source of the MOS

type transistor S2 is connected to the level address line X1, and the gate is connected to the perpendicular address line Y1. The gate of a transistor S1 is connected to the transistor S2.

[0027] The data line DL1 is connected to the input of the buffer B1 of number of input impedances 100komega. The output of a buffer B1 is connected to an output line OL through the transistor Q1 for output selection. The gate of a transistor Q1 is connected to the level address line X1. The output line OL is connected to the output terminal P through output-buffer alumnus. The data line DL2 is similarly connected to the output line OL through the transistor Q1 of a buffer B1 and an MOS type.

[0028] Next, operation is explained. The charge by which photo electric translation was carried out according to the amount of incident lights is accumulated at Photodiode D. First, if the perpendicular address line Y1 and the level address line X1 are chosen, the gate of a transistor S2 will become highness and will carry out a turn-on. Since the source of a transistor S2 is also highness, the charge by which the gate of a transistor S1 became highness, and the turn-on was carried out, and it was stored in Photodiode D is distributed to the data line DL1. At this time, since the gate is connected to the level address line X1, the transistor Q1 for output selection has also been turned on [it], and the charge on the data line DL1 is read to an output line OL through a buffer B1 and a transistor Q1.

[0029] If one of the perpendicular address line Y1 and the level address lines X1 is not chosen, a bird clapper does not have the gate of a transistor S1 in highness. That is, MOS transistor S1 is controlled by the compound address (x1, y1) with which the level address x1 and the perpendicular address y1 were doubled.

[0030] Moreover, since the data line DL2 flows into the direction of a buffer B1 immediately even if a noise charge is incorporated, since the input impedance is connected to the low buffer B1, a noise charge is not accumulated at the data line DL2. Furthermore, since the data line DL2 is separated from the output line OL by the transistor Q1, the parasitic capacitance connected to an output line OL becomes the small thing of only a transistor Q1. Moreover, by making the output impedance of a buffer B1 low, making a transistor Q1 approach, and arranging, between a buffer B1 and transistors Q1 is maintained at a low impedance, and it can prevent gathering a noise charge.

[0031] this example is constituted as mentioned above, and since the transistor S1 which connects Photodiode D to the data lines DL1 and DL2 and ... is controlled by the compound address (x1, y1) of the level address x1 and the perpendicular address y1, random access becomes possible. Moreover, since the data line is connected to the low buffer B1 of an input impedance, the data line of the train which is not accessed is maintained at a low impedance, and can prevent generating of aliases, such as a smear and shading.

[0032] Furthermore, since the transistor Q1 for output selection is connected with the buffer B1 between output lines OL, the parasitic capacitance of an output line OL is small, and a speed of response also becomes quick. Therefore, random access is possible, and an alias can be prevented and image sensors also with a quick speed of response are obtained.

[0033] In addition, although the data line is arranged to the perpendicular address line and parallel in this example As it is not limited to this, for example, is shown in drawing 2 , arrange data-line DL'1 and DL'2 to the perpendicular address line and parallel, and it connects with a buffer B'1. The flexibility on a design can be raised by controlling by the perpendicular address line, and arranging the data line aslant or arranging the transistor Q'1 for output selection wavelike.

[0034] Next, the 2nd example of this invention is explained using drawing 3 and drawing 4 . Drawing 3 is drawing showing the composition of this example. Drawing 4 is the timing chart explaining operation of address selection. The pixel FC2 connected to the perpendicular address line Y1 and the level address line X1 like the 1st example is taken for an example, and the composition is explained. A pixel FC2 consists of resistance R1 connected with MOS type transistor S4 allotted between the gates

of the transistor S3 MOS type [for a switch] which connects to the data line alternatively the photodiode D which is a photo detector, and a photodiode, and the level address line X1 and a transistor S3 at the gate of a transistor S3. The gate of transistor S4 is connected to the perpendicular address line Y1.

[0035] The data line DL1 is connected to the input of the buffer B1 of number of input impedances 100komega. The output of a buffer B1 is connected to an output line OL by Adder OA. And the output line OL is connected to the output terminal P through output-buffer alumnus. Similarly, the data line DL2 is also connected with the buffer B1 through Adder OA to the output line OL.

[0036] In order to explain operation of a pixel FC2, operation when Resistance R is not connected probably is explained. If resistance R1 is not connected to the pixel FC2, the charge of the photodiode D of the pixel is outputted to an output line OL by choosing the level address line X1 and the perpendicular address line Y1 which are connected to the pixel concerned like the example 1 shown in drawing 1 . In choosing the specific pixel FC2, whichever they choose previously, there is no trouble of the level address line X1 and the Y1 perpendicular address line in operation. However, although the turn-off of the transistor S3 will be carried out if the level address line X1 will be in the state where it does not choose, previously when returning to the state where it does not choose from a selection state, and it is convenient in operation, if the perpendicular address line Y1 will be previously returned to the state where it does not choose, transistor S4 will carry out a turn-off, and the gate of the level address line X1 and a transistor S3 will be intercepted.

[0037] Even if it makes the level address line X1 un-choosing after that, the gate charge of a transistor S3 will remain and it will stop therefore, as for a transistor S3, being able to carry out the turn-off of it. Therefore, as shown in drawing 4 , after making level address-line X (X1, X2, ...) un-choosing first, you have to make perpendicular address-line Y (Y1, Y2, ...) un-choosing.

[0038] On the other hand, since the charge of a transistor S3 can escape through resistance R1 even if the perpendicular address line Y1 will be in the state where it does not choose, previously and transistor S4 carries out a turn-off, since resistance R1 becomes the recess path of the charge of a transistor S3 when resistance R1 is connected, a transistor S3 can carry out a turn-off. That is, if resistance R1 is connected, restrictions of the control timing when returning the address line to the state where it does not choose, from a selection state will be lost. Resistance R1 forms a pull-up circuit, when a transistor S3 is a transistor of P type, and when a transistor S3 is N type, it serves as a pulldown circuit.

[0039] Adder OA adds the output of a buffer B1 to an output line OL. Only the information on a pixel that the pixel was chosen as the output line OL since one was chosen by the perpendicular address and the level address is read. In addition, although a transistor S3 may fully be unable to turn on the potential of the gate of a transistor S3 even if transistor S4 carries out the turn-on of it since it is the potential which deducted the threshold of transistor S4 from potential when the level address is chosen, it can carry out the turn-on of the transistor S3 certainly beforehand in that case by carrying out the pressure up of the potential when the level address is chosen by methods, such as a bootstrap. Other composition and operation are the same as that of the 1st example shown in drawing 1 .

[0040] this example is constituted as mentioned above, first, by having added resistance R1 to the pixel FC2, it is prevented that a transistor S3 will not carry out a turn-off, and restrictions of the control timing when returning the address line to the state where it does not choose, from a selection state are lost. Moreover, since the data line and the output line are separated by constituting a readout circuitry from a buffer and an adder OA, it becomes unnecessary to extend the level address line to the output of a buffer B1, and a circuit is simplified. Therefore, while the same effect as the 1st example is acquired, there are no restrictions of control timing and the effect that a circuit is simplified is

acquired.

[0041] Next, the 3rd example which read and changed the composition of the section is explained. Drawing 5 shows the whole block diagram and drawing 6 shows the circuit diagram of the read-out section. In this example, a pixel is the 2nd thing and this composition of an example. The read-out section consists of buffer B-2s which showed the detail to drawing 6 . buffer B-2 -- the data line DL1 -- hundreds -- the gate of the end of the k-ohm resistance R2 and the MOSFET type transistor T1 is connected, and the drain of a transistor T1 serves as an output of buffer B-2 The other end of resistance R2 is grounded. The source of a transistor T1 is also grounded and a transistor T1 is a grounded-source type transistor. Resistance 3 is connected to the output line OL.

[0042] In this example, the charge of a pixel FC2 is read to the data line DL1, and if the read charge flows resistance R2 from the data line DL1 in buffer B-2, it will be transformed into voltage. The changed voltage is impressed to the gate of a transistor T1. The current which flows a transistor T1 is proportional to the gate voltage, i.e., the voltage changed by resistance R2. Current is transformed into voltage by the resistance R3 by which the current proportional to the current which flows the data line DL1 flows an output line OL, and is connected to an output line OL, and serves as an output by it.

[0043] At buffer B-2, since resistance R2 is connected to the data line DL1, there is no bird clapper of the DL1 data line in high impedance, and the input impedance of buffer B-2 is a low. Moreover, a transistor T1 is a grounded-source type transistor, and that of the impedance of the transistor T1 seen from the drain is high, and since it is set to dozens of M omega or more, the output impedance of buffer B-2 becomes high.

[0044] For this reason, even if it connects the output of direct buffer B-2 to an output line OL, the current proportional to the current which flows the data line which the output of each buffer B-2 became multi-input OR connection on the output line OL, and was connected to the selected pixel FC2 flows an output line OL. And it hardly leaks to other buffer B-2s, and the current which flows an output line OL is transformed into voltage, and serves as an output. Other composition and operation are the same as that of the 2nd example shown in drawing 3 .

[0045] While the same effect as the 2nd example is acquired by this, since the data line DL and an output line OL are connectable, a circuit is further simplified only by buffer B-2. In addition, in each above-mentioned example, although it read and the section was explained, it is not limited to this but read-out sensitivity can also be raised by [equipped with the buffer / equipped with amplifier] reading and using the section.

[0046] Next, the 4th example of this invention which changed the composition of the read-out section is explained. Drawing 7 is the circuit diagram of the read-out section in this example. The pixel sections are the 2nd, and the 3rd example and this composition. The read-out section consists of buffers B3. a buffer B3 -- the data line DL1 -- hundreds -- it connects with the gate of the end of the k-ohm resistance R4, and the MOSFET type transistor T2 The other end of resistance R4 and the source of a transistor T2 are grounded. The drain of a transistor T2 is connected to the source of the MOSFET type transistor T3. The gate of a transistor T3 is connected to the fixed potential lines floor line, such as grounding. The drain of a transistor T3 serves as an output of a buffer B3, and is connected to the output line OL. The MOSFET type transistor Q2 by which diode connection was made is connected to the output line OL.

[0047] In this example, current is transformed into voltage by the transistor Q2 by which the current which is proportional to the current which flows the data line DL1 with resistance R4 and the transistor T2 of a buffer B3 flows an output line OL, and is connected to an output line OL, and serves as an output with it. Since resistance R4 is connected to the data line DL1 in the buffer B3, there is no bird clapper of the DL1 data line in high impedance, and the input impedance of a buffer B3 is a low.

Moreover, a transistor T2 and a transistor T3 constitute a cascode circuit, and the impedance seen from the drain of a transistor T3 is larger than the impedance seen from the drain of a transistor T2.

[0048] For this reason, even if the output impedance of a buffer B3 becomes still higher and it connects the output of the direct buffer B3 to an output line OL, the output of each buffer B3 serves as multi-input OR connection, and the current proportional to the current which flows the data line DL1 flows an output line OL, is transformed into voltage, and serves as an output. Moreover, the speed of response as a buffer also improves by cascode connection. Furthermore, since the transistor Q2 by which diode connection was made is used for the output line OL instead of resistance, amplification degree also improves. since the output impedance of a buffer B3 is still larger while the same effect as the 3rd example is acquired by this, the current-potential conversion precision in an output line improves, and a speed of response becomes still quicker again

[0049] Drawing 8 is the circuit diagram of the read-out section of the 5th example of this invention which changed the composition of the read-out section. At this example, it reads and the section consists of buffers B4. In the buffer B4, the data line DL1 is connected to MOSFET type the gate and the drain of a transistor T5 by which diode connection was made while connecting with the gate of the MOSFET type transistor T4. Furthermore, the current source I is connected to these nodes. The source of a transistor T5 is connected to fixed potential. It is grounded, the drain of a transistor T4 serves as an output of a buffer B4, and the source of a transistor T4 is connected to the output line OL. The pixel section is the 1st example and this composition.

[0050] In this example, in the buffer B4, a transistor T4 and a transistor T5 constitute current Miller circuit, and bias is carried out by the current source I. Since the current proportional to the current which the current which flows the data line DL1 flows a transistor T5, and flows a transistor T5 flows T4, the current proportional to the current which flows the data line DL1 flows an output line OL, and is changed and outputted to voltage. Since the drain, the gate, and the current source I of a transistor T5 are connected to the data line DL1 in the buffer B4, there is no bird clapper of the DL1 data line in high impedance, and the input impedance of a buffer B4 is a low.

[0051] Moreover, a transistor T5 and a transistor T4 constitute current Miller circuit, and even if the output impedance of current Miller circuit is high and it carries out the direct file of the output of a buffer B4 to an output line OL, the output of each buffer B4 serves as multi-input OR connection. The current proportional to the current which flows the data line DL1 flows an output line OL, is transformed into voltage, and serves as an output. Other composition and operation are the same as that of the 4th example, and the transistor Q2 by which diode connection was made is connected to the output line OL.

[0052] Since the ejection precision of current becomes good by use of current Miller circuit while the same effect as the 3rd example is acquired by this, output precision improves. In addition, by this example, although current Miller circuit was used, it does not restrict to this, cascode current Miller circuit and the Wilson type current Miller circuit are sufficient, and if a cascode circuit is combined, current-potential conversion precision and a speed of response will improve.

[0053] Drawing 9 is the circuit diagram of the read-out section of the 6th example of this invention which changed the composition of the read-out section. At this example, it reads and the section consists of buffer B5. The data line DL1 is connected to the source of the MOSFET type transistor T6 in buffer B5. The gate of a transistor T6 is connected to the fixed potential line floor line, and the drain is connected to the output line OL. The transistor Q3 MOSFET type [for loads] is connected to the output line OL. Other composition is the same as the 1st and the 5th example.

[0054] In this example, a transistor T6 is a grounded-gate type transistor circuit, and the current which flows the data line DL1 flows to an output line through the source and the drain of a transistor T6. In

buffer B5, since the impedance of the transistor T6 seen from the source of a transistor T6 is low, there is no data line DL1 in high impedance with a bird clapper, and the input impedance of buffer B5 has it. [low]

[0055] Moreover, since the impedance of the transistor T6 seen from the drain of a transistor T6 is high, even if it carries out the direct file of the output of buffer B5 to an output line OL, the output of each buffer B5 serves as multi-input OR connection. The current proportional to the current which flows the data line DL1 by this flows an output line OL, is transformed into voltage with a transistor Q3, and serves as an output. Furthermore, since a grounded-gate circuit has the source current and equal drain current and its current ejection precision is good, there are few constituent children and it is good with one transistor. Moreover, since there is also no delay of the signal by the Miller effect, a speed of response is also quick. While the same effect as the 3rd example was acquired by this, improvement and the circuit were further simplified for output precision by use of a grounded-gate type transistor, and the speed of response improved more.

[0056] Next, the 7th example of this invention which changed the composition of a pixel is explained. Drawing 10 is the circuit diagram of the pixel of this example. A pixel FC3 consists of MOS transistor S5 for the switch which connects to the data line alternatively the photodiode D which is a photo detector, and a photodiode, MOS transistor S6 connected to the perpendicular address line, S7 which is a switch for a frame transfer, and a transistor S8 which is a switch for reset of a photodiode.

[0057] The source of MOS transistor S6 is connected to the level address line X1, and the gate is connected to the perpendicular address line Y1, respectively. The gate of a transistor S5 is connected to the drain of MOS transistor S6. The transistor S7 is connected to Photodiode D and the transistor S8. The frame shift signal FS is inputted into the gate of a transistor S7, and reset-signal RS is inputted into the gate of a transistor S8. Moreover, the remaining electrodes of a transistor S8 are connected to reset potential.

[0058] In this example, the compound address is generated by the transistor S6 and the data line DL1 is connected with Photodiode D by the transistor S5. Moreover, if the frame shift signal FS is inputted into the gate of a transistor S7, the charge of each pixel FC3 will be transmitted. Furthermore, if reset-signal RS is inputted into a transistor S8, the anode of Photodiode D will be connected to reset potential, and Photodiode D will be reset. In addition, the composition of the read-out section is the same also in the 6th example of drawing 9 .

[0059] A frame transfer is attained while the same effect as the 1st example is acquired by this. Moreover, reset of Photodiode D is attained, an electronic shutter can be realized, and much more practical convenience improves. In addition, in each above-mentioned example, although the cathode of Photodiode D is connected to fixed potential, it may not be limited to this, but an anode may be connected to fixed potential, and one of the electrodes of Photodiode D should just be connected to fixed potential.

[0060] Drawing 11 is the circuit diagram of the pixel of the example of the octavus of this invention which changed the composition of a pixel. In the pixel FC4 of this example, the anode of the photodiode D which is a photo detector is connected to the data line DL1 through MOS transistor S9 for a switch, and the cathode is connected to fixed potential through MOS transistor S10. The gate of transistor S9 is connected to the perpendicular address line Y1, and the gate of a transistor S10 is connected to the level address line X1.

[0061] In this example, when using insulating substrates, such as SOI, for a substrate, the photoelectrical load of a pixel of transistor S9 and a transistor S10 with which generation of the compound address and the function of both selection operation of data-line connection were simultaneously achieved, respectively, and horizontal / vertical address line was chosen

simultaneously is sent out without the need of connecting Photodiode D to fixed potential to the data line DL1. The read-out sections are the 6th, and the 7th example and this composition.

[0062] Since there is no need of connecting Photodiode D to fixed potential while the same effect as the 1st example is acquired by this, in case the flexibility on a design improves and it is used as pixels, such as an image processing,-izing of the pixel can be carried out [detailed] and the resolution of a picture can be raised. In addition, in the example of the 7th octavus, although it read, and it was the same as the 6th example and the composition of the section was explained, the effect of the addition explained for every example can be acquired by combining with the composition and arbitration of the read-out section in each the 1st to 5th example.

[0063]

[Effect of the Invention] Since the switching means by which this invention connects a photo detector to the data line as above are controlled by the compound address of the level address and the perpendicular address, random access becomes possible. Moreover, since the data line is connected to the output line through a read-out means to have a low input impedance, the data line is maintained at a low impedance and the parasitic capacitance of an output line does not increase, a smear and shading are also prevented.

[0064] In addition, by attaching a charge electric discharge means to the 1st switching means which connect a photo detector to the data line alternatively, at the time of un-choosing [of the level address line and the perpendicular address line], the charge which remains in the 1st switching means discharges, and it is not concerned in order of the non-choosing change of the level address line and the perpendicular address line, but the effect of being intercepted certainly is acquired.

[0065] Moreover, when a read-out means is equipped with an output selection means or an addition means between a buffer or amplifier, and an output line, the parasitic capacitance of an output line becomes small and a speed of response also becomes quick. Furthermore, when a read-out means shall have the buffer or amplifier which has a low input impedance and a high power impedance, the direct file of the output of the buffer or amplifier can be carried out to an output line, and the image sensors by which the circuit was simplified are obtained.

TECHNICAL FIELD

[The technical field to which invention belongs] This invention relates to the image sensors which used the photo detector.

PRIOR ART

[Description of the Prior Art] As conventional image sensors, there is a thing as shown in drawing 12 , for example. Two or more pixel FC5a which consists of transistors S11 MOS type [for a switch] which connect alternatively to the data line the photodiode D these image sensors of whose are photo detectors, and a photodiode, FC5b, FC5c, and FC5d are arranged in the shape of two-dimensional.

[0003] Pixel FC5a corresponding to the level address line X1 and the perpendicular address line Y1 is taken for an example, and the composition is explained. Photodiode D is connected to the data line DL1 through the transistor S11. The gate of a transistor S11 is connected to the perpendicular address line Y1. The data line DL1 is connected to the output line OL through the transistor Q4 MOS type [

for a switch] which connects this data line DL1 to an output line OL alternatively. The output line OL is connected to the output terminal P through output-buffer alumnus. The gate of a transistor Q4 is connected to the level address line X1. The perpendicular address line Y1 and the level address line X1 are connected to the perpendicular address scanning circuit YD and the level address scanning circuit XD which consist of a shift register, respectively.

[0004] In these image sensors, the charge by which photo electric translation was carried out to the period when the transistor S11 is turned off according to the amount of incident lights is accumulated at Photodiode D. First, if the level address line X1 is chosen as the degree by which the charge accumulated by turning on [it] a transistor S11 at Photodiode D will be distributed to the data line DL1 if the perpendicular address line Y1 is chosen, a transistor Q4 will be turned on [it], the data line DL1 is connected with an output line OL, and the charge of the data line DL1 is sent to output-buffer alumnus through an output line OL. Thereby, the charge stored in Photodiode D can be read.

EFFECT OF THE INVENTION

[Effect of the Invention] Since the switching means by which this invention connects a photo detector to the data line as above are controlled by the compound address of the level address and the perpendicular address, random access becomes possible. Moreover, since the data line is connected to the output line through a read-out means to have a low input impedance, the data line is maintained at a low impedance and the parasitic capacitance of an output line does not increase, a smear and shading are also prevented.

[0064] In addition, by attaching a charge electric discharge means to the 1st switching means which connect a photo detector to the data line alternatively, at the time of un-choosing [of the level address line and the perpendicular address line], the charge which remains in the 1st switching means discharges, and it is not concerned in order of the non-choosing change of the level address line and the perpendicular address line, but the effect of being intercepted certainly is acquired.

[0065] Moreover, when a read-out means is equipped with an output selection means or an addition means between a buffer or amplifier, and an output line, the parasitic capacitance of an output line becomes small and a speed of response also becomes quick. Furthermore, when a read-out means shall have the buffer or amplifier which has a low input impedance and a high power impedance, the direct file of the output of the buffer or amplifier can be carried out to an output line, and the image sensors by which the circuit was simplified are obtained.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, there was a problem that aliases, such as a smear and shading, occurred, in such conventional image sensors. First, a smear is explained. As for the photodiode of the line connected to the perpendicular address line, all are connected to each data line while the perpendicular address line is chosen. For example, the charge stored in the photodiode D of pixel FC5c is also distributed to the data line DL2 at the same time the charge stored in the photodiode D of pixel FC5a will be distributed to the data line DL1, if the perpendicular address line Y1 is chosen in order to read the charge of the photodiode D of pixel FC5a. On the other hand, since the transistor Q4 which connects the data line DL2 and an output line OL turns off, the data line DL2 is in the high

impedance state. Therefore, the distributed charge will be stored in the data line DL2, and the potential of the data line DL2 will rise.

[0006] If the quantity of light which carried out incidence to the photodiode D of pixel FC5c is large, since there are also many the charges, the potential of the data line DL2 becomes high, the threshold of the transistor S11 of other pixel FC5d linked to the data line DL2 is exceeded, it will become impossible to maintain an OFF state, the charge in the data line DL2 will leak to the photodiode D of pixel FC5d through a transistor S11, and the transistor S11 will be accumulated.

[0007] This phenomenon is called saturation of the data line and causes a smear. It becomes the picture which the smear SU as if a light strong against all the pixels of the train carried out [if the data line was not saturated,] incidence as shown in (b) of drawing 13 when a picture as shown in (a) of drawing 13 was acquired, and the data line of the train of the light source H was saturated generated. In addition, the smear is the same, even if an MOS transistor also generates P type or N type and the photodiode is operating in solar-battery mode. Although using it, lowering the dynamic range is performed in order to prevent generating of a smear, if it does so, since a range is insufficient, sufficient picture will no longer be acquired at the time of photography or photography of night.

[0008] Next, shading is explained. When there is no incident light in all the photodiodes D when using image sensors in the pitch-black state, and read-out is performed, shading may occur. The perpendicular address line Y1 is chosen first, and, next, read-out is chosen in order of the level address lines X1 and X2. In case the transistor S11 of pixel FC5a and the transistor Q4 connected to the data line DL1 turn on, a charge is supplied from the exterior, a part of supplied charge passes along the parasitic capacitance between the gate and a substrate, and it leaks to a substrate. The charge which leaked to the substrate is injected into the source and the drain of a transistor S11 in pixel FC5c or pixel FC5d by capacity coupling and diffusion.

[0009] Since the transistor Q4 connected to the data line DL2 at this time turns off, the data line DL2 is in the high impedance state, and the leaked charge is stored in the data line DL2 linked to the source of S11. Next, if the data line DL2 is chosen, the transistor Q4 connected to DL2 will be turned on [it], and the stored leakage charge will be read as an alias. Since the leakage charge is added as the scan of the address line progresses, the picture turns into a picture which the luminosity increases by the scanning direction of **** as shown in (c) of drawing 13 .

[0010] Furthermore, in case these image sensors are used for an image processing, they have the problem that random access cannot be done. That is, in case an image processing is performed, the random access function which reads arbitrary pixels in arbitrary turn is required. However, in these conventional image sensors, read-out is divided into two stages, and is performed, perpendicular address-line Y is chosen first, and the charge stored in the photodiode D of the line is distributed to the data line DL connected, respectively. Next, level address-line X is chosen and each charge of DL is read to an output line OL.

[0011] For example, when reading the charge of the photodiode D of FC5a, the charge of the photodiode D of FC5c will also be distributed to the data line DL2. Next, first, if it is going to read the charge of the photodiode D of FC5d, in order to throw away the charge of the data line DL2, dummy read-out must be performed once and the data line DL2 must be reset. If the photodiode D of FC5d is read, the charge of the photodiode D of FC5c will be thrown away and, next, the charge of the photodiode D of FC5c cannot be read.

[0012] Therefore, this invention aims at being able to prevent generating of aliases, such as a smear and shading, and offering the image sensors in which random access is possible in view of the above-mentioned conventional trouble.

MEANS

[Means for Solving the Problem] For this reason, this invention according to claim 1 is arranged at a plane, is chosen by the level address line and the perpendicular address line, and is set to image sensors equipped with two or more pixels connected to the data line. It has the switching means which connect a photo detector to the data line when both the level address line corresponding to a photo detector and the pixel concerned in each of a pixel and the perpendicular address line are chosen. The data line shall be connected to an output line through a read-out means to have a low input impedance.

[0014] The 1st switching means by which the above-mentioned switching means connect a photo detector to the data line alternatively, It consists of the 2nd switching means which turn ON the 1st switching means when both the level address line and the perpendicular address line are chosen. The 2nd switching means consist of transistors and the gate of a transistor is connected to either the level address line or the perpendicular address line. One side of electrodes other than the gate shall be connected to another side of the level address line or the perpendicular address line, and the electrode of another side shall be connected to the 1st switching means.

[0015] It is desirable to attach further a charge electric discharge means to discharge the charge which remains in the 1st switching means at the time of un-choosing [of the level address line and the perpendicular address line] to the 1st switching means. Moreover, the above-mentioned photo detector is made into a photodiode, the 1st switching means are constituted from a transistor, and while connecting the gate of this transistor with the 2nd switching means, connecting one side of electrodes other than the gate to a photodiode and connecting the electrode of another side to the data line, a charge electric discharge means can constitute the gate of the 1st switching means from the resistance or the current source linked to fixed potential.

[0016] A pixel invention according to claim 5, respectively Moreover, the photodiode as a photo detector, The 1st transistor which connects the anode of this photodiode to the data line, While having the 2nd transistor which connects a cathode to fixed potential and connecting the gate of the 1st transistor to either the level address line or the perpendicular address line The gate of the 2nd transistor shall be connected to another side of the level address line and the perpendicular address line, and the data line shall be connected to an output line through a read-out means to have a low input impedance. •

[0017] In each invention, the above-mentioned read-out means can consist of the buffer or amplifier which has a low input impedance, and an output selection means to allow the output of a buffer or amplifier, and connection of an output line only when a photo detector is connected to the data line linked to the read-out means concerned.

[0018] Or a read-out means shall have the buffer or amplifier which has a low input impedance and a high power impedance, and shall carry out the direct file of the output of the buffer or amplifier to an output line again. Under the present circumstances, the buffer or amplifier of a low input impedance and a high power impedance shall be equipped with grounded-source type a transistor circuit, current Miller circuit, or a grounded-gate type transistor circuit.

OPERATION

[Function] In the thing of a claim 1, in each pixel, switching means connect the photo detector of the pixel concerned to the data line, when both the level address line and the perpendicular address line are chosen. That is, since a transistor S12 is arranged as switching means which connect a photo detector and the data lines, such as Photodiode D, and these switching means are controlled by the compound address (xi-yj) (i= 1, 2, ..., j= 1, 2, ...) of the perpendicular address and the level address to be shown in drawing 14 , each pixel can be read independently and random access becomes possible.

[0020] By the way, if the direct file of the data line and the output line is carried out, the new problem that the parasitic capacitance of an output line increases will arise. That is, if all the data lines are connected to an output line, the parasitic capacitance of the switch in all pixels will work as a parasitic capacitance of an output line, the parasitic capacitance of an output line will become large, and a speed of response will become slow. For example, when there are the 512x512 numbers of pixels, the parasitic capacitance of the switch for 512x512 pieces is connected to the data line. In the conventional example, since the switch linked to an output line is 512x2 pieces, the parasitic capacitance of an output line becomes a bird clapper to (512x512) / (512x2) =256 time of the parasitic capacitance of the conventional example.

[0021] In this invention, since the data line is connected to the output line through a read-out means to have a low input impedance, a bird clapper is prevented for the data line by high impedance, and the parasitic capacitance of an output line does not increase. Since a bird clapper does not have the data line in high impedance, a smear and shading are also prevented.

[0022] In addition, it is simply constituted using a transistor, respectively by dividing switching means into the 1st switching means and 2nd switching means. Moreover, by attaching the charge electric discharge means of connecting the gate of the transistor to fixed potential by resistance etc. to the 1st switching means which connect a photo detector to the data line alternatively, at the time of un-choosing [of the level address line and the perpendicular address line], the charge which remains in the 1st switching means discharges, and it is not concerned in order of the non-choosing change of the level address line and the perpendicular address line, but is intercepted certainly.

[0023] Moreover, when a read-out means shall have the buffer or amplifier which has a low input impedance and a high power impedance, even if it carries out the direct file of the output of the buffer or amplifier to an output line, the output of other pixels does not flow backwards from an output-line side.

[0024] In the thing of a claim 5, since the two poles of the photodiode as a photo detector of each pixel are connected to the 1st transistor and 2nd transistor and it is not necessary to connect with fixed potential, constituting on an insulating substrate is easy.

[0025]

[Embodiments of the Invention] An example explains the form of implementation of invention. Drawing 1 is drawing showing the 1st example of this invention. The n level address lines X1-Xn connected to the m perpendicular address lines Y1-Ym by which these image sensors were connected to the perpendicular address scanning circuit YD, and the level address scanning circuit XD are arranged in the shape of a grid, and the n data lines DL1-DLn are arranged together with the level address lines X1-Xn. A pixel FC1 consists of MOS type transistors S2 connected at MOS type the transistor S1 and the perpendicular address line for the switch which connects to the data line alternatively the photodiode D which is a photo detector, and a photodiode.

[0026] The pixel FC1 of an mxn individual is arranged in the shape of two-dimensional, and each pixel FC1 is controlled by the perpendicular address y on the perpendicular address line, and the level address x on the level address line. In order to simplify explanation, the image sensors in m= 2 and n= 2 are shown in drawing 1 . The pixel FC1 connected to the perpendicular address line Y1 and the level

address line X1 is taken for an example, and the composition is explained. The source of the MOS type transistor S2 is connected to the level address line X1, and the gate is connected to the perpendicular address line Y1. The gate of a transistor S1 is connected to the transistor S2.

[0027] The data line DL1 is connected to the input of the buffer B1 of number of input impedances 100komega. The output of a buffer B1 is connected to an output line OL through the transistor Q1 for output selection. The gate of a transistor Q1 is connected to the level address line X1. The output line OL is connected to the output terminal P through output-buffer alumnus. The data line DL2 is similarly connected to the output line OL through the transistor Q1 of a buffer B1 and an MOS type.

[0028] Next, operation is explained. The charge by which photo electric translation was carried out according to the amount of incident lights is accumulated at Photodiode D. First, if the perpendicular address line Y1 and the level address line X1 are chosen, the gate of a transistor S2 will become highness and will carry out a turn-on. Since the source of a transistor S2 is also highness, the charge by which the gate of a transistor S1 became highness, and the turn-on was carried out, and it was stored in Photodiode D is distributed to the data line DL1. At this time, since the gate is connected to the level address line X1, the transistor Q1 for output selection has also been turned on [it], and the charge on the data line DL1 is read to an output line OL through a buffer B1 and a transistor Q1.

[0029] If one of the perpendicular address line Y1 and the level address lines X1 is not chosen, a bird clapper does not have the gate of a transistor S1 in highness. That is, MOS transistor S1 is controlled by the compound address (x1, y1) with which the level address x1 and the perpendicular address y1 were doubled.

[0030] Moreover, since the data line DL2 flows into the direction of a buffer B1 immediately even if a noise charge is incorporated, since the input impedance is connected to the low buffer B1, a noise charge is not accumulated at the data line DL2. Furthermore, since the data line DL2 is separated from the output line OL by the transistor Q1, the parasitic capacitance connected to an output line OL becomes the small thing of only a transistor Q1. Moreover, by making the output impedance of a buffer B1 low, making a transistor Q1 approach, and arranging, between a buffer B1 and transistors Q1 is maintained at a low impedance, and it can prevent gathering a noise charge.

[0031] this example is constituted as mentioned above, and since the transistor S1 which connects Photodiode D to the data lines DL1 and DL2 and ... is controlled by the compound address (x1, y1) of the level address x1 and the perpendicular address y1, random access becomes possible. Moreover, since the data line is connected to the low buffer B1 of an input impedance, the data line of the train which is not accessed is maintained at a low impedance, and can prevent generating of aliases, such as a smear and shading.

[0032] Furthermore, since the transistor Q1 for output selection is connected with the buffer B1 between output lines OL, the parasitic capacitance of an output line OL is small, and a speed of response also becomes quick. Therefore, random access is possible, and an alias can be prevented and image sensors also with a quick speed of response are obtained.

[0033] In addition, although the data line is arranged to the perpendicular address line and parallel in this example As it is not limited to this, for example, is shown in drawing 2 , arrange data-line DL'1 and DL'2 to the perpendicular address line and parallel, and it connects with a buffer B'1. The flexibility on a design can be raised by controlling by the perpendicular address line, and arranging the data line aslant or arranging the transistor Q'1 for output selection wavelike.

[0034] Next, the 2nd example of this invention is explained using drawing 3 and drawing 4 . Drawing 3 is drawing showing the composition of this example. Drawing 4 is the timing chart explaining operation of address selection. The pixel FC2 connected to the perpendicular address line Y1 and the level address line X1 like the 1st example is taken for an example, and the composition is explained. A

pixel FC2 consists of resistance R1 connected with MOS type transistor S4 allotted between the gates of the transistor S3 MOS type [for a switch] which connects to the data line alternatively the photodiode D which is a photo detector, and a photodiode, and the level address line X1 and a transistor S3 at the gate of a transistor S3. The gate of transistor S4 is connected to the perpendicular address line Y1.

[0035] The data line DL1 is connected to the input of the buffer B1 of number of input impedances 100komega. The output of a buffer B1 is connected to an output line OL by Adder OA. And the output line OL is connected to the output terminal P through output-buffer alumnus. Similarly, the data line DL2 is also connected with the buffer B1 through Adder OA to the output line OL.

[0036] In order to explain operation of a pixel FC2, operation when Resistance R is not connected probably is explained. If resistance R1 is not connected to the pixel FC2, the charge of the photodiode D of the pixel is outputted to an output line OL by choosing the level address line X1 and the perpendicular address line Y1 which are connected to the pixel concerned like the example 1 shown in drawing 1 . In choosing the specific pixel FC2, whichever they choose previously, there is no trouble of the level address line X1 and the Y1 perpendicular address line in operation. However, although the turn-off of the transistor S3 will be carried out if the level address line X1 will be in the state where it does not choose, previously when returning to the state where it does not choose from a selection state, and it is convenient in operation, if the perpendicular address line Y1 will be previously returned to the state where it does not choose, transistor S4 will carry out a turn-off, and the gate of the level address line X1 and a transistor S3 will be intercepted.

[0037] Even if it makes the level address line X1 un-choosing after that, the gate charge of a transistor S3 will remain and it will stop therefore, as for a transistor S3, being able to carry out the turn-off of it. Therefore, as shown in drawing 4 , after making level address-line X (X1, X2, ...) un-choosing first, you have to make perpendicular address-line Y (Y1, Y2, ...) un-choosing.

[0038] On the other hand, since the charge of a transistor S3 can escape through resistance R1 even if the perpendicular address line Y1 will be in the state where it does not choose, previously and transistor S4 carries out a turn-off, since resistance R1 becomes the recess path of the charge of a transistor S3 when resistance R1 is connected, a transistor S3 can carry out a turn-off. That is, if resistance R1 is connected, restrictions of the control timing when returning the address line to the state where it does not choose, from a selection state will be lost. Resistance R1 forms a pull-up circuit, when a transistor S3 is a transistor of P type, and when a transistor S3 is N type, it serves as a pulldown circuit.

[0039] Adder OA adds the output of a buffer B1 to an output line OL. Only the information on a pixel that the pixel was chosen as the output line OL since one was chosen by the perpendicular address and the level address is read. In addition, although a transistor S3 may fully be unable to turn on the potential of the gate of a transistor S3 even if a transistor S4 carries out the turn-on of it since it is the potential which deducted the threshold of a transistor S4 from potential when the level address is chosen, it can carry out the turn-on of the transistor S3 certainly beforehand in that case by carrying out the pressure up of the potential when the level address is chosen by methods, such as a bootstrap. Other composition and operation are the same as that of the 1st example shown in drawing 1 .

[0040] this example is constituted as mentioned above, first, by having added resistance R1 to the pixel FC2, it is prevented that a transistor S3 will not carry out a turn-off, and restrictions of the control timing when returning the address line to the state where it does not choose, from a selection state are lost. Moreover, since the data line and the output line are separated by constituting a readout circuitry from a buffer and an adder OA, it becomes unnecessary to extend the level address line to the output of a buffer B1, and a circuit is simplified. Therefore, while the same effect as the 1st example is

acquired, there are no restrictions of control timing and the effect that a circuit is simplified is acquired.

[0041] Next, the 3rd example which read and changed the composition of the section is explained. Drawing 5 shows the whole block diagram and drawing 6 shows the circuit diagram of the read-out section. In this example, a pixel is the 2nd thing and this composition of an example. The read-out section consists of buffer B-2s which showed the detail to drawing 6 . buffer B-2 -- the data line DL1 -- hundreds -- the gate of the end of the k-ohm resistance R2 and the MOSFET type transistor T1 is connected, and the drain of a transistor T1 serves as an output of buffer B-2 The other end of resistance R2 is grounded. The source of a transistor T1 is also grounded and a transistor T1 is a grounded-source type transistor. Resistance 3 is connected to the output line OL.

[0042] In this example, the charge of a pixel FC2 is read to the data line DL1, and if the read charge flows resistance R2 from the data line DL1 in buffer B-2, it will be transformed into voltage. The changed voltage is impressed to the gate of a transistor T1. The current which flows a transistor T1 is proportional to the gate voltage, i.e., the voltage changed by resistance R2. Current is transformed into voltage by the resistance R3 by which the current proportional to the current which flows the data line DL1 flows an output line OL, and is connected to an output line OL, and serves as an output by it.

[0043] At buffer B-2, since resistance R2 is connected to the data line DL1, there is no bird clapper of the DL1 data line in high impedance, and the input impedance of buffer B-2 is a low. Moreover, a transistor T1 is a grounded-source type transistor, and that of the impedance of the transistor T1 seen from the drain is high, and since it is set to dozens of M omega or more, the output impedance of buffer B-2 becomes high.

[0044] For this reason, even if it connects the output of direct buffer B-2 to an output line OL, the current proportional to the current which flows the data line which the output of each buffer B-2 became multi-input OR connection on the output line OL, and was connected to the selected pixel FC2 flows an output line OL. And it hardly leaks to other buffer B-2s, and the current which flows an output line OL is transformed into voltage, and serves as an output. Other composition and operation are the same as that of the 2nd example shown in drawing 3 .

[0045] While the same effect as the 2nd example is acquired by this, since the data line DL and an output line OL are connectable, a circuit is further simplified only by buffer B-2. In addition, in each above-mentioned example, although it read and the section was explained, it is not limited to this but read-out sensitivity can also be raised by [equipped with the buffer / equipped with amplifier] reading and using the section.

[0046] Next, the 4th example of this invention which changed the composition of the read-out section is explained. Drawing 7 is the circuit diagram of the read-out section in this example. The pixel sections are the 2nd, and the 3rd example and this composition. The read-out section consists of buffers B3. a buffer B3 -- the data line DL1 -- hundreds -- it connects with the gate of the end of the k-ohm resistance R4, and the MOSFET type transistor T2 The other end of resistance R4 and the source of a transistor T2 are grounded. The drain of a transistor T2 is connected to the source of the MOSFET type transistor T3. The gate of a transistor T3 is connected to the fixed potential lines floor line, such as grounding. The drain of a transistor T3 serves as an output of a buffer B3, and is connected to the output line OL. The MOSFET type transistor Q2 by which diode connection was made is connected to the output line OL.

[0047] In this example, current is transformed into voltage by the transistor Q2 by which the current which is proportional to the current which flows the data line DL1 with resistance R4 and the transistor T2 of a buffer B3 flows an output line OL, and is connected to an output line OL, and serves as an output with it. Since resistance R4 is connected to the data line DL1 in the buffer B3, there is no

bird clapper of the DL1 data line in high impedance, and the input impedance of a buffer B3 is a low. Moreover, a transistor T2 and a transistor T3 constitute a cascode circuit, and the impedance seen from the drain of a transistor T3 is larger than the impedance seen from the drain of a transistor T2.

[0048] For this reason, even if the output impedance of a buffer B3 becomes still higher and it connects the output of the direct buffer B3 to an output line OL, the output of each buffer B3 serves as multi-input OR connection, and the current proportional to the current which flows the data line DL1 flows an output line OL, is transformed into voltage, and serves as an output. Moreover, the speed of response as a buffer also improves by cascode connection. Furthermore, since the transistor Q2 by which diode connection was made is used for the output line OL instead of resistance, amplification degree also improves. since the output impedance of a buffer B3 is still larger while the same effect as the 3rd example is acquired by this, the current-potential conversion precision in an output line improves, and a speed of response becomes still quicker again

[0049] Drawing 8 is the circuit diagram of the read-out section of the 5th example of this invention which changed the composition of the read-out section. At this example, it reads and the section consists of buffers B4. In the buffer B4, the data line DL1 is connected to MOSFET type the gate and the drain of a transistor T5 by which diode connection was made while connecting with the gate of the MOSFET type transistor T4. Furthermore, the current source I is connected to these nodes. The source of a transistor T5 is connected to fixed potential. It is grounded, the drain of a transistor T4 serves as an output of a buffer B4, and the source of a transistor T4 is connected to the output line OL. The pixel section is the 1st example and this composition.

[0050] In this example, in the buffer B4, a transistor T4 and a transistor T5 constitute current Miller circuit, and bias is carried out by the current source I. Since the current proportional to the current which the current which flows the data line DL1 flows a transistor T5, and flows a transistor T5 flows T4, the current proportional to the current which flows the data line DL1 flows an output line OL, and is changed and outputted to voltage. Since the drain, the gate, and the current source I of a transistor T5 are connected to the data line DL1 in the buffer B4, there is no bird clapper of the DL1 data line in high impedance, and the input impedance of a buffer B4 is a low.

[0051] Moreover, a transistor T5 and a transistor T4 constitute current Miller circuit, and even if the output impedance of current Miller circuit is high and it carries out the direct file of the output of a buffer B4 to an output line OL, the output of each buffer B4 serves as multi-input OR connection. The current proportional to the current which flows the data line DL1 flows an output line OL, is transformed into voltage, and serves as an output. Other composition and operation are the same as that of the 4th example, and the transistor Q2 by which diode connection was made is connected to the output line OL.

[0052] Since the ejection precision of current becomes good by use of current Miller circuit while the same effect as the 3rd example is acquired by this, output precision improves. In addition, by this example, although current Miller circuit was used, it does not restrict to this, cascode current Miller circuit and the Wilson type current Miller circuit are sufficient, and if a cascode circuit is combined, current-potential conversion precision and a speed of response will improve.

[0053] Drawing 9 is the circuit diagram of the read-out section of the 6th example of this invention which changed the composition of the read-out section. At this example, it reads and the section consists of buffer B5. The data line DL1 is connected to the source of the MOSFET type transistor T6 in buffer B5. The gate of a transistor T6 is connected to the fixed potential line floor line, and the drain is connected to the output line OL. The transistor Q3 MOSFET type [for loads] is connected to the output line OL. Other composition is the same as the 1st and the 5th example.

[0054] In this example, a transistor T6 is a grounded-gate type transistor circuit, and the current which

flows the data line DL1 flows to an output line through the source and the drain of a transistor T6. For the impedance of the transistor T6 seen from the source of a transistor T6 in buffer B5, for a low reason, there is no bird clapper in high impedance, and the input impedance of buffer B5 is [the data line DL1] a low.

[0055] Moreover, since the impedance of the transistor T6 seen from the drain of a transistor T6 is high, even if it carries out the direct file of the output of buffer B5 to an output line OL, the output of each buffer B5 serves as multi-input OR connection. The current proportional to the current which flows the data line DL1 by this flows an output line OL, is transformed into voltage with a transistor Q3, and serves as an output. Furthermore, since a grounded-gate circuit has the source current and equal drain current and its current ejection precision is good, there are few constituent children and it is good with one transistor. Moreover, since there is also no delay of the signal by the Miller effect, a speed of response is also quick. While the same effect as the 3rd example was acquired by this, improvement and the circuit were further simplified for output precision by use of a grounded-gate type transistor, and the speed of response improved more.

[0056] Next, the 7th example of this invention which changed the composition of a pixel is explained. Drawing 10 is the circuit diagram of the pixel of this example. A pixel FC3 consists of MOS transistor S5 for the switch which connects to the data line alternatively the photodiode D which is a photo detector, and a photodiode, MOS transistor S6 connected to the perpendicular address line, S7 which is a switch for a frame transfer, and a transistor S8 which is a switch for reset of a photodiode.

[0057] The source of MOS transistor S6 is connected to the level address line X1, and the gate is connected to the perpendicular address line Y1, respectively. The gate of a transistor S5 is connected to the drain of MOS transistor S6. The transistor S7 is connected to Photodiode D and the transistor S8. The frame shift signal FS is inputted into the gate of a transistor S7, and reset-signal RS is inputted into the gate of a transistor S8. Moreover, the remaining electrodes of a transistor S8 are connected to reset potential.

[0058] In this example, the compound address is generated by the transistor S6 and the data line DL1 is connected with Photodiode D by the transistor S5. Moreover, if the frame shift signal FS is inputted into the gate of a transistor S7, the charge of each pixel FC3 will be transmitted. Furthermore, if reset-signal RS is inputted into a transistor S8, the anode of Photodiode D will be connected to reset potential, and Photodiode D will be reset. In addition, the composition of the read-out section is the same also in the 6th example of drawing 9 .

[0059] A frame transfer is attained while the same effect as the 1st example is acquired by this. Moreover, reset of Photodiode D is attained, an electronic shutter can be realized, and much more practical convenience improves. In addition, in each above-mentioned example, although the cathode of Photodiode D is connected to fixed potential, it may not be limited to this, but an anode may be connected to fixed potential, and one of the electrodes of Photodiode D should just be connected to fixed potential.

[0060] Drawing 11 is the circuit diagram of the pixel of the example of the octavus of this invention which changed the composition of a pixel. In the pixel FC4 of this example, the anode of the photodiode D which is a photo detector is connected to the data line DL1 through MOS transistor S9 for a switch, and the cathode is connected to fixed potential through MOS transistor S10. The gate of transistor S9 is connected to the perpendicular address line Y1, and the gate of a transistor S10 is connected to the level address line X1.

[0061] In this example, when using insulating substrates, such as SOI, for a substrate, the photoelectrical load of a pixel of transistor S9 and a transistor S10 with which generation of the compound address and the function of both selection operation of data-line connection were

simultaneously achieved, respectively, and horizontal / vertical address line was chosen simultaneously is sent out without the need of connecting Photodiode D to fixed potential to the data line DL1. The read-out sections are the 6th, and the 7th example and this composition.

[0062] Since there is no need of connecting Photodiode D to fixed potential while the same effect as the 1st example is acquired by this, in case the flexibility on a design improves and it is used as pixels, such as an image processing,-izing of the pixel can be carried out [detailed] and the resolution of a picture can be raised. In addition, in the example of the 7th octavus, although it read, and it was the same as the 6th example and the composition of the section was explained, the effect of the addition explained for every example can be acquired by combining with the composition and arbitration of the read-out section in each the 1st to 5th example.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is drawing showing the 1st example of this invention.

[Drawing 2] It is drawing showing the modification of data-line arrangement.

[Drawing 3] It is drawing showing the 2nd example.

[Drawing 4] It is explanatory drawing of address selection timing.

[Drawing 5] It is drawing showing the 3rd example.

[Drawing 6] It is the circuit diagram of the read-out section of the 3rd example.

[Drawing 7] It is drawing showing the 4th example.

[Drawing 8] It is drawing showing the 5th example.

[Drawing 9] It is drawing showing the 6th example.

[Drawing 10] It is drawing showing the 7th example.

[Drawing 11] It is drawing showing the example of the octavus.

[Drawing 12] It is drawing showing the conventional example.

[Drawing 13] It is drawing explaining the problem in the conventional example.

[Drawing 14] It is explanatory drawing of the compound address.

[Description of Notations]

B1, B'1, B-2, B3 and B4, B5 Buffer

D Photodiode (photo detector)

DL1, DL2, DL'1, DL'2 Data line

FC1, FC2, FC3, FC4, FC5 Pixel

H Light source

I Current source

OA Adder (addition means)

alumnus Output buffer

OL Output line

P Output terminal

Q1, Q'1 Transistor (output selection means)

Q2, Q3, Q4 Transistor

R1 Resistance (charge electric discharge means)

R2, R3, R4 Resistance

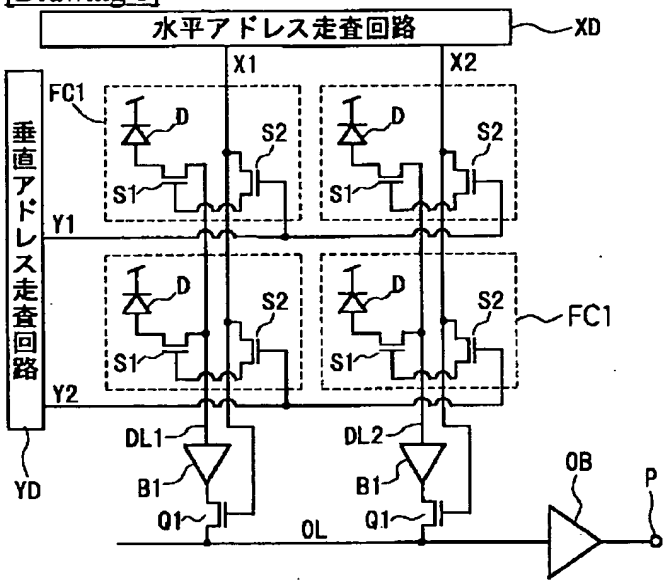
S1, S3, S5 Transistor (the 1st switching means)

S2, S4, S6 Transistor (the 2nd switching means)

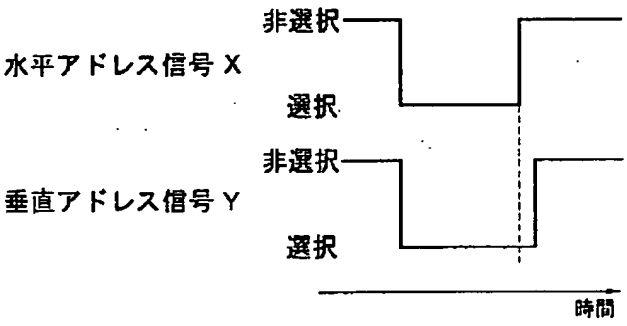
S7, S8 Transistor
S9 Transistor (the 1st transistor)
S10 Transistor (the 2nd transistor)
S12 Transistor (switching means)
SU Smear
T1, T2, T3, T4, T5, T6 Transistor
X1, X2 Level address line
XD Level address scanning circuit
Y1, Y2 Perpendicular address line
YD Perpendicular address scanning circuit

DRAWINGS

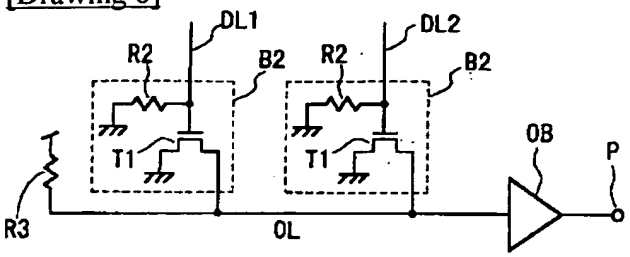
[Drawing 1]



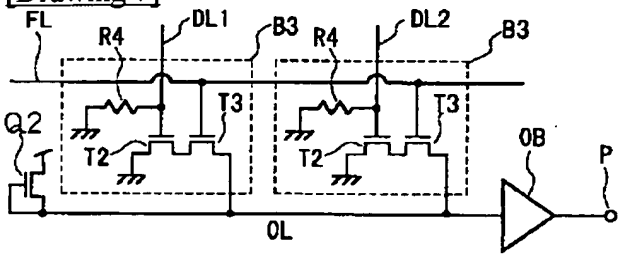
[Drawing 4]



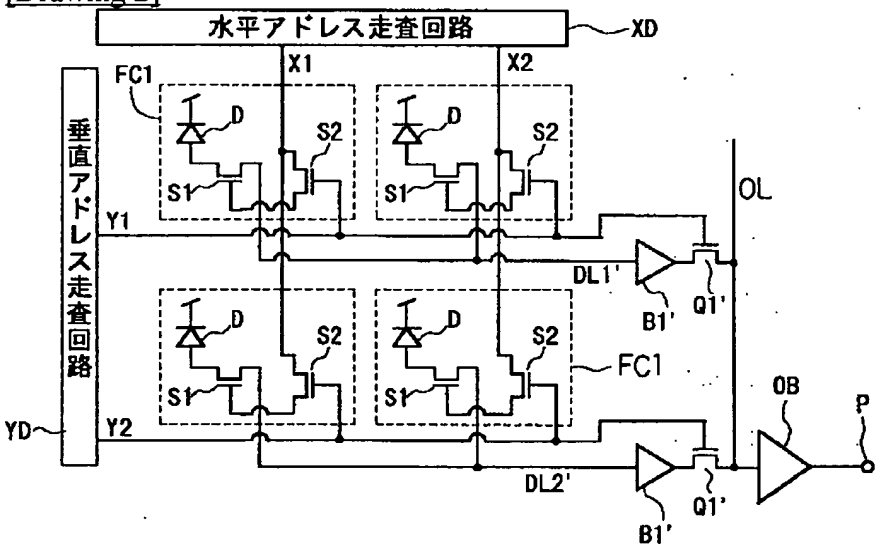
[Drawing 6]



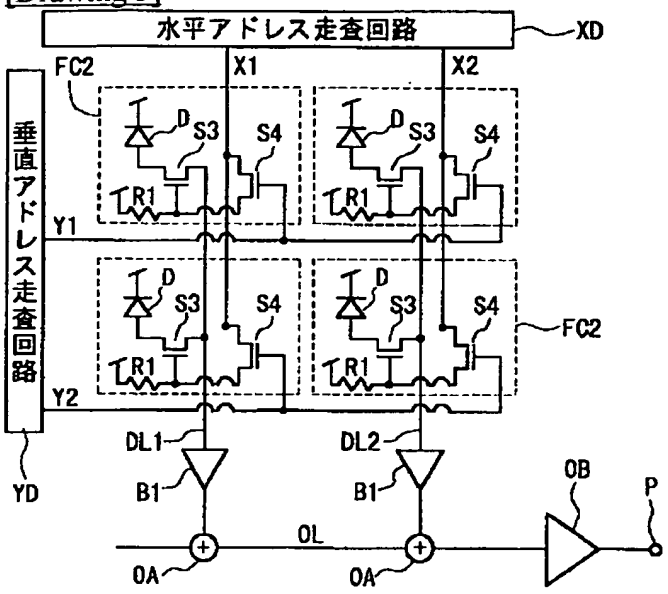
[Drawing 7]



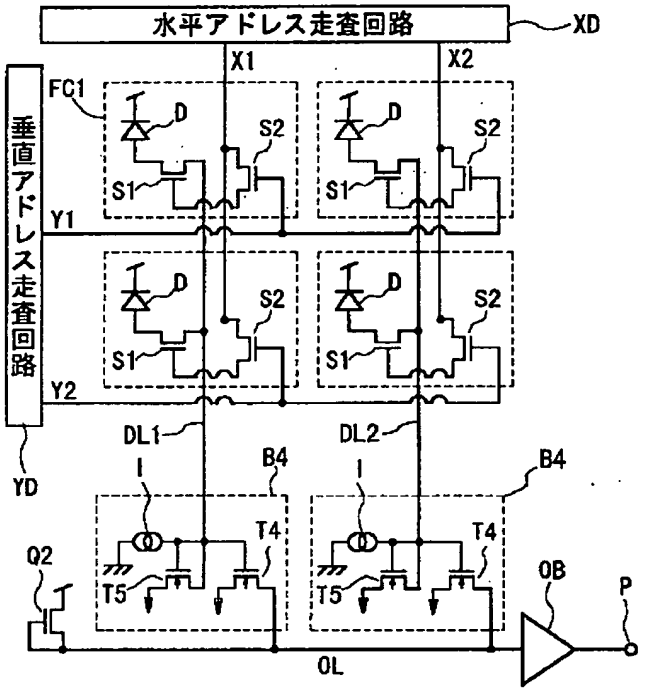
[Drawing 2]



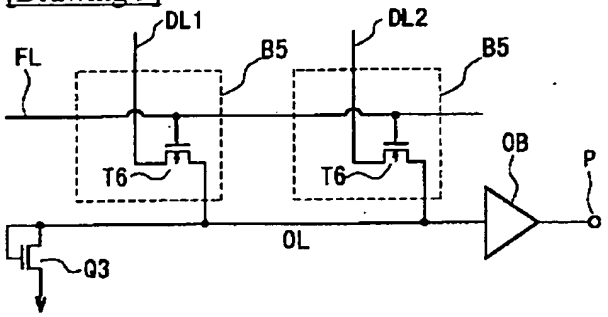
[Drawing 3]



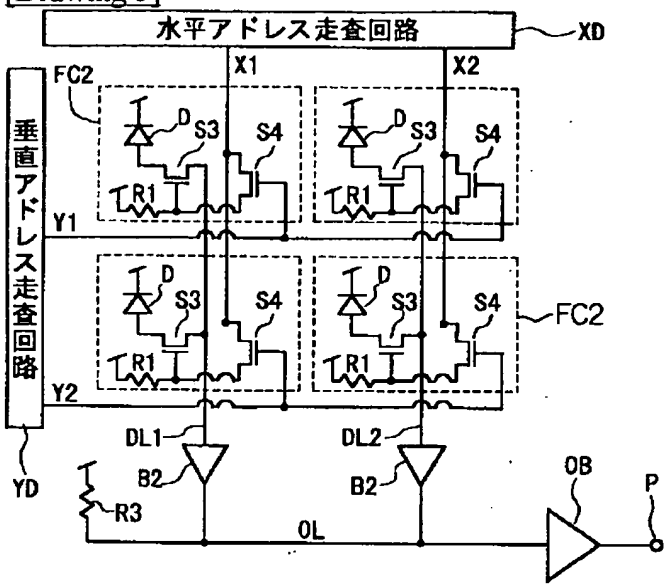
[Drawing 8]



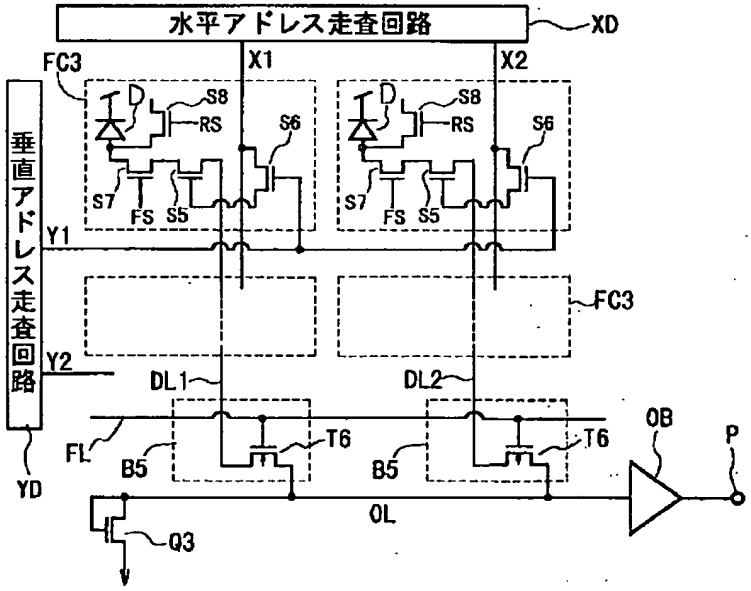
[Drawing 9]



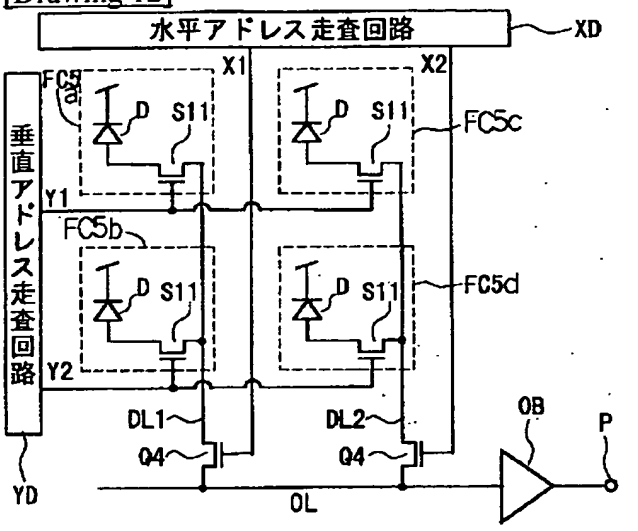
[Drawing 5]



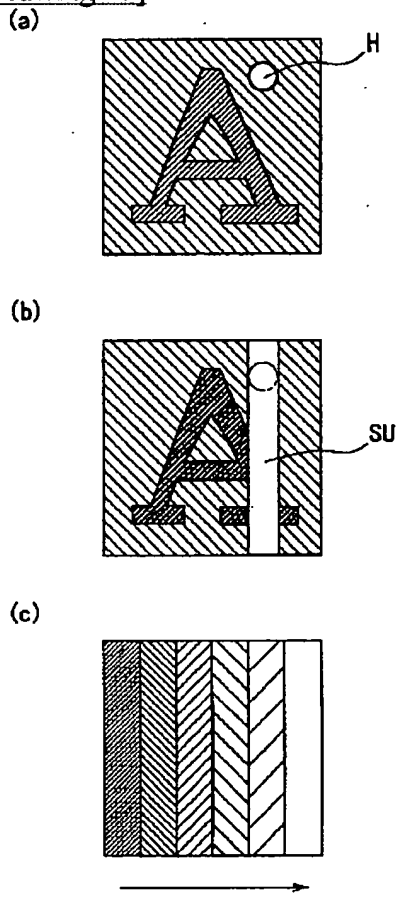
[Drawing 10]



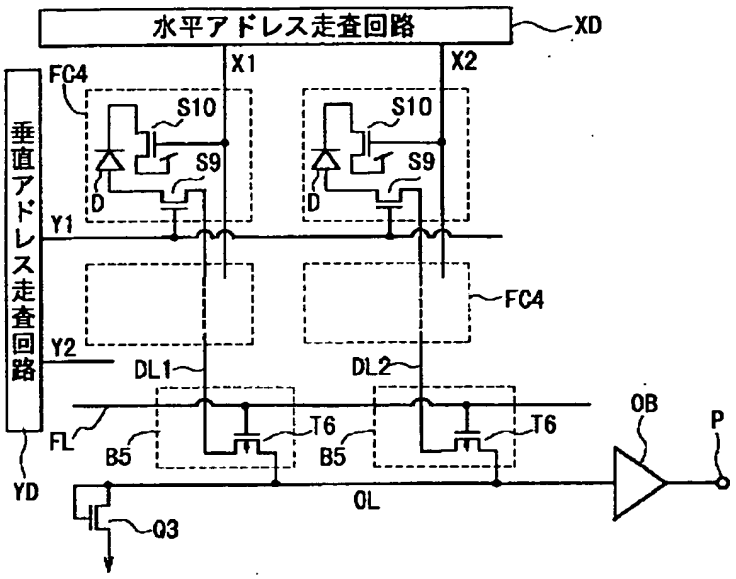
[Drawing 12]



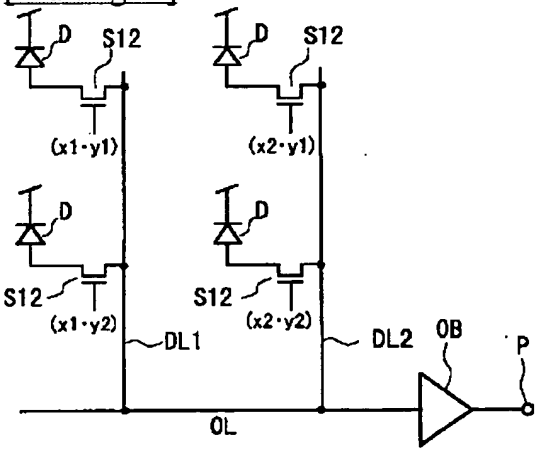
[Drawing 13]



[Drawing 11]



[Drawing 14]



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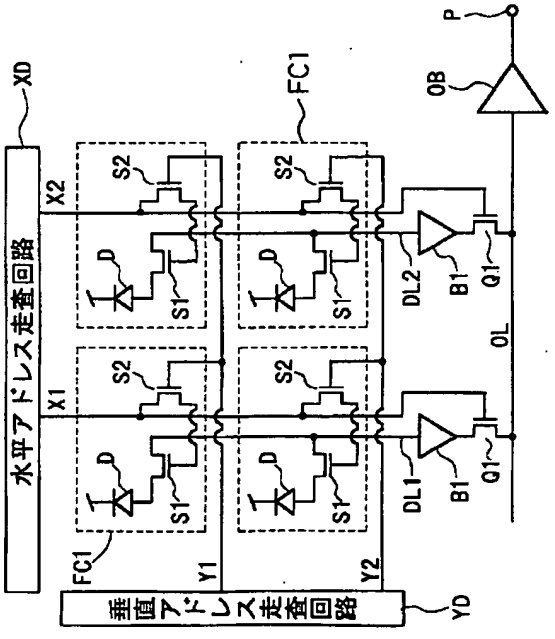
(54)【発明の名称】　イメージセンサ

(57)【要約】

【課題】　スミアやシェーディングなどの偽信号の発生を防止する。

【解決手段】　フォトダイオードＤがトランジスタＳ１を介してデータ線ＤＬ１に接続され、また水平アドレス線Ｘ１に接続されてトランジスタＳ１を制御するトランジスタＳ２のゲートが垂直アドレス線に接続されている。データ線は低入力インピーダンスのバッファＢ１に入力接続し、バッファの出力はトランジスタＱ１を介して出力線ＯＬに出力される。　垂直アドレス線Ｙ１と水平アドレス線Ｘ１が選択されるとトランジスタＳ２がターンオンし、これによりトランジスタＳ１がターンオンして、フォトダイオードＤに蓄えられた電荷がデータ線ＤＬ１に送出され，トランジスタＱ１を経て送出される。雑音電荷は入力インピーダンスが低いバッファＢ１の方へ流れ出すからデータ線に蓄積されず、偽信号の発生が抑えられる。



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【特許請求の範囲】

【請求項1】　平面状に配置され、水平アドレス線および垂直アドレス線により選択され、データ線に接続される複数の画素を備えたイメージセンサにおいて、前記画素のそれぞれが受光素子と、当該画素に対応する水平アドレス線および垂直アドレス線の両方が選択されたとき前記受光素子をデータ線に接続するスイッチ手段と、前記データ線と出力線との間に接続され、前記データ線側が低入力インピーダンスの読み出し手段とを有することを特徴とするイメージセンサ。

【請求項2】　前記スイッチ手段が、受光素子を選択的にデータ線に接続する第1のスイッチ手段と、水平アドレス線および垂直アドレス線の両方が選択されたときに前記第1のスイッチ手段をオンにする第2のスイッチ手段とからなり、該第2のスイッチ手段がトランジスタから構成され、該トランジスタのゲートが水平アドレス線または垂直アドレス線の一方に接続され、ゲート以外の電極の一方が水平アドレス線または垂直アドレス線の他方に接続され、他方の電極が前記第1のスイッチ手段のゲートに接続されていることを特徴とする請求項1記載のイメージセンサ。

【請求項3】　前記第1のスイッチ手段には、水平アドレス線および垂直アドレス線の非選択時に第1のスイッチ手段に残存する電荷を放電する電荷放電手段が付設されていることを特徴とする請求項2記載のイメージセンサ。

【請求項4】　前記受光素子がフォトダイオードであり、前記第1のスイッチ手段がトランジスタから構成され、該トランジスタのゲートが前記第2のスイッチ手段と接続され、ゲート以外の電極の一方が前記フォトダイオードに接続され、他方の電極が前記データ線に接続されるとともに、前記電荷放電手段が第1のスイッチ手段の前記ゲートを固定電位に接続する抵抗または電流源からなることを特徴とする請求項3記載のイメージセンサ。

【請求項5】　平面状に配置され、水平アドレス線および垂直アドレス線により選択され、データ線に接続される複数の画素を備えたイメージセンサにおいて、前記画素のそれぞれが、フォトダイオードからなる受光素子と、該フォトダイオードのアノードをデータ線に接続する第1のトランジスタと、カソードを固定電位に接続する第2のトランジスタとを備え、前記第1のトランジスタのゲートが水平アドレス線および垂直アドレス線の一方に接続されるとともに、第2のトランジスタのゲートが水平アドレス線および垂直アドレス線の他方に接続され、前記データ線が低入力インピーダンスを有する読み出し手段を介して出力線に接続されていることを特徴とするイメージセンサ。

【請求項6】　前記読み出し手段が、低入力インピーダンスを有するバッファまたは増幅器と、当該読み出し手段に接続するデータ線に前記受光素子が接続されたときに前記バッファまたは増幅器の出力と出力線を接続する出力選択手段または加算手段とから構成されていることを特徴とする請求項1、2、3、4または5記載のイメージセンサ。

【請求項7】　前記読み出し手段が、低入力インピーダンスおよび高出力インピーダンスを有するバッファまたは増幅器を有し、該バッファまたは増幅器の出力が前記出力線に直接接続されていることを特徴とする請求項1、2、3、4または5記載のイメージセンサ。

【請求項8】　前記バッファまたは増幅器がソース接地型のトランジスタ回路を備えることを特徴とする請求項7記載のイメージセンサ。

【請求項9】　前記バッファまたは増幅器がカレント・ミラー回路を備えることを特徴とする請求項7記載のイメージセンサ。

【請求項10】　前記バッファまたは増幅器がゲート接地型トランジスタ回路を備えることを特徴とする請求項7記載のイメージセンサ。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】この発明は、受光素子を用いたイメージセンサに関する。

【0002】

【従来の技術】従来のイメージセンサとしては、例えば、図12に示すようなものがある。このイメージセンサは、受光素子であるフォトダイオードDとフォトダイオードを選択的にデータ線に接続するスイッチ用のMOS型のトランジスタS11から構成される複数の画素FC5a、FC5b、FC5c、FC5dが2次元状に配置されている。

【0003】水平アドレス線X1と垂直アドレス線Y1に対応する画素FC5aを例にとり、その構成を説明する。フォトダイオードDは、トランジスタS11を介してデータ線DL1に接続されている。トランジスタS11のゲートは、垂直アドレス線Y1に接続されている。データ線DL1は、このデータ線DL1を選択的に出力線OLに接続するスイッチ用のMOS型のトランジスタQ4を介して、出力線OLに接続されている。出力線OLは、出力バッファOBを介して出力端子Pに接続されている。トランジスタQ4のゲートは、水平アドレス線X1に接続されている。垂直アドレス線Y1および水平アドレス線X1は、それぞれシフトレジスタからなる垂直アドレス走査回路YDおよび水平アドレス走査回路XDに接続されている。

【0004】このイメージセンサでは、トランジスタS11がオフされている期間に、入射光量に応じて光電変換された電荷がフォトダイオードDに蓄積される。まず、垂直アドレス線Y1が選択されると、トランジスタS11がオンになり、フォトダイオードDに蓄積された

電荷がデータ線ＤＬ１に分配される、次に水平アドレス線Ｘ１が選択されるとトランジスタＱ４がオンになり、データ線ＤＬ１は出力線ＯＬと接続され、データ線ＤＬ１の電荷は出力線ＯＬを介して出力バッファＯＢへ送られる。これにより、フォトダイオードＤに蓄えられた電荷を読み出すことができる。

【０００５】

【発明が解決しようとする課題】しかしながらこのような従来のイメージセンサでは、スミアやシェーディング等の偽信号が発生するという問題があった。まず、スミアについて説明する。垂直アドレス線が選択されている間は、その垂直アドレス線に接続されている行のフォトダイオードはすべてが、それぞれのデータ線に接続される。例えば、画素ＦＣ５ａのフォトダイオードＤの電荷を読み出すために垂直アドレス線Ｙ１を選択すると、画素ＦＣ５ａのフォトダイオードＤに蓄えられた電荷がデータ線ＤＬ１に分配されると同時に、画素ＦＣ５ｃのフォトダイオードＤに蓄えられた電荷もデータ線ＤＬ２に分配される。一方、データ線ＤＬ２と出力線ＯＬを接続するトランジスタＱ４がオフしているので、データ線ＤＬ２は、ハイ・インピーダンス状態になっている。したがって、分配された電荷がデータ線ＤＬ２に蓄えられ、データ線ＤＬ２の電位が上昇することになる。

【０００６】画素ＦＣ５ｃのフォトダイオードＤに入射した光量が大きいと、その電荷も多いため、データ線ＤＬ２の電位が高くなり、データ線ＤＬ２に接続している他の画素ＦＣ５ｄのトランジスタＳ１１のしきい値を越えてしまい、そのトランジスタＳ１１はオフ状態を保てなくなり、データ線ＤＬ２内の電荷がトランジスタＳ１１を通して画素ＦＣ５ｄのフォトダイオードＤへ漏れ、蓄積される。

【０００７】この現象はデータ線の飽和と呼ばれ、スミアの原因となる。データ線が飽和していなければ、図１３の（ａ）に示すような画像が得られる場合に、光源Ｈの列のデータ線が飽和すると、図１３の（ｂ）に示すように、あたかもその列のすべての画素に強い光が入射したかのようなスミアＳＵが発生した画像になる。なお、ＭＯＳトランジスタがＰ型でもＮ型でもスミアは発生し、また、フォトダイオードが太陽電池モードで動作していても同様である。スミアの発生を予防するため、ダイナミック・レンジを下げて使用することが行われているが、そうすると、野外撮影や夜間の撮影のときに、レンジ不足のため十分な画像が得られなくなる。

【０００８】次に、シェーディングについて説明する。真っ暗な状態でイメージセンサを使用した時等の、全てのフォトダイオードＤに入射光がない場合に、読み出しが行われるとシェーディングが発生することがある。読み出しは、まず垂直アドレス線Ｙ１が選択され、次に水平アドレス線Ｘ１、Ｘ２の順で選択される。画素ＦＣ５ａのトランジスタＳ１１やデータ線ＤＬ１に接続されているトランジスタＱ４がオンする際、外部から電荷が供給され、供給された電荷の一部が、ゲート・基板間の寄生容量を通って、基板へ漏れる。基板へ漏れた電荷は、容量結合や拡散によって画素ＦＣ５ｃや画素ＦＣ５ｄ内のトランジスタＳ１１のソースおよびドレインに注入される。

【０００９】この時データ線ＤＬ２に接続されているトランジスタＱ４がオフしているから、データ線ＤＬ２がハイ・インピーダンス状態になっており、漏れた電荷はＳ１１のソースに接続しているデータ線ＤＬ２に蓄えられる。次に、データ線ＤＬ２が選択されると、ＤＬ２に接続されているトランジスタＱ４がオンになり、蓄えられた漏れ電荷が偽信号として読み出される。アドレス線の走査が進むにつれて、漏れ電荷が加算されていくため、その画像は図１３の（ｃ）に示すような矢示の走査方向で明るさが増加していく画像となる。

【００１０】さらに、このイメージセンサは、画像処理に用いる際にランダムアクセスができないという問題がある。すなわち、画像処理を行う際には、任意の画素を任意の順番で読み出すランダムアクセス機能が必要である。しかし、この従来のイメージセンサでは、読み出しが２段階に分かれて行われ、まず垂直アドレス線Ｙが選択され、その行のフォトダイオードＤに蓄えられた電荷がそれぞれ接続されたデータ線ＤＬに分配される。次に水平アドレス線Ｘが選択され、それぞれのＤＬの電荷が出力線ＯＬに読みだされる。

【００１１】例えば、ＦＣ５ａのフォトダイオードＤの電荷を読み出す時に、ＦＣ５ｃのフォトダイオードＤの電荷もデータ線ＤＬ２に分配されてしまう。次に、ＦＣ５ｄのフォトダイオードＤの電荷を読みだそうとすると、まず、データ線ＤＬ２の電荷を捨てる為に、一回ダミー読み出しを行い、データ線ＤＬ２をリセットしなければならない。ＦＣ５ｄのフォトダイオードＤを読み出すと、ＦＣ５ｃのフォトダイオードＤの電荷が捨てられてしまい、次にＦＣ５ｃのフォトダイオードＤの電荷を読み出すことができない。

【００１２】したがって本発明は上記従来の問題点に鑑み、スミアやシェーディングなどの偽信号の発生を防止でき、また、ランダムアクセスが可能なイメージセンサを提供することを目的とする。

【００１３】

【課題を解決するための手段】このため、請求項１記載の本発明は、平面状に配置され、水平アドレス線および垂直アドレス線により選択され、データ線に接続される複数の画素を備えたイメージセンサにおいて、画素のそれぞれが受光素子と、当該画素に対応する水平アドレス線および垂直アドレス線の両方が選択されたとき受光素子をデータ線に接続するスイッチ手段を備え、データ線が低入力インピーダンスを有する読み出し手段を介して出力線に接続されているものとした。

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【００１４】上記スイッチ手段は、受光素子を選択的にデータ線に接続する第１のスイッチ手段と、水平アドレス線および垂直アドレス線の両方が選択されたときに第１のスイッチ手段をオンにする第２のスイッチ手段とからなり、第２のスイッチ手段がトランジスタから構成され、トランジスタのゲートが水平アドレス線または垂直アドレス線の一方に接続され、ゲート以外の電極の一方が水平アドレス線または垂直アドレス線の他方に接続され、他方の電極が第１のスイッチ手段に接続されているものとすることができる。

【００１５】第１のスイッチ手段には、さらに、水平アドレス線および垂直アドレス線の非選択時に第１のスイッチ手段に残存する電荷を放電する電荷放電手段を付設するのが好ましい。また、上記の受光素子をフォトダイオードとし、第１のスイッチ手段をトランジスタで構成し、このトランジスタのゲートを第２のスイッチ手段と接続し、ゲート以外の電極の一方をフォトダイオードに接続し、他方の電極をデータ線に接続するとともに、電荷放電手段は第１のスイッチ手段のゲートを固定電位に接続する抵抗または電流源から構成することができる。

【００１６】また、請求項５記載の発明は、画素のそれぞれが、受光素子としてのフォトダイオードと、このフォトダイオードのアノードをデータ線に接続する第１のトランジスタと、カソードを固定電位に接続する第２のトランジスタとを備え、第１のトランジスタのゲートが水平アドレス線および垂直アドレス線の一方に接続されるとともに、第２のトランジスタのゲートが水平アドレス線および垂直アドレス線の他方に接続され、データ線が低入力インピーダンスを有する読み出し手段を介して出力線に接続されているものとした。

【００１７】各発明において、上記読み出し手段は、低入力インピーダンスを有するバッファまたは増幅器と、当該読み出し手段に接続するデータ線に受光素子が接続されたときのみバッファまたは増幅器の出力と出力線の接続を許す出力選択手段とから構成することができる。

【００１８】あるいはまた、読み出し手段は、低入力インピーダンスおよび高出力インピーダンスを有するバッファまたは増幅器を有し、そのバッファまたは増幅器の出力を出力線に直接接続するものとすることもできる。この際、低入力インピーダンスおよび高出力インピーダンスのバッファまたは増幅器は、ソース接地型のトランジスタ回路、カレント・ミラー回路、あるいはゲート接地型トランジスタ回路を備えるものとすることができる。

【００１９】

【作用】請求項１のものでは、各画素において、スイッチ手段が水平アドレス線および垂直アドレス線の両方が選択されたとき当該画素の受光素子をデータ線に接続する。すなわち、図１４に示すように、例えばフォトダイオードＤなどの受光素子とデータ線を接続するスイッチ

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手段として例えばトランジスタＳ１２を配置し、このスイッチ手段を垂直アドレスと水平アドレスの複合アドレス（ｘｉ・ｙｊ）（ｉ＝１、２、・・・、ｊ＝１、２、・・・）で制御するので、各画素を独立に読み出せ、ランダムアクセスが可能になる。

【００２０】ところで、データ線と出力線を直接接続すると、出力線の寄生容量が増大するという新たな問題が生じる。すなわち、総てのデータ線が出力線に接続されれば、総ての画素内のスイッチの寄生容量が出力線の寄生容量として働き、出力線の寄生容量が大きくなり、応答速度が遅くなってしまう。例えば、画素数が５１２×５１２個ある場合には、５１２×５１２個分のスイッチの寄生容量がデータ線に接続される。従来例では出力線に接続するスイッチは５１２×２個であるので、出力線の寄生容量は、従来例の寄生容量の（５１２×５１２）／（５１２×２）＝２５６倍になることになる。

【００２１】本発明ではデータ線が低入力インピーダンスを有する読み出し手段を介して出力線に接続されているので、データ線がハイ・インピーダンスになることが防止され、出力線の寄生容量が増大しない。データ線がハイ・インピーダンスになることがないため、スミアやシェーディングも防止される。

【００２２】なお、スイッチ手段を第１のスイッチ手段と第２のスイッチ手段に分けることにより、それぞれトランジスタを用いて簡単に構成される。また、受光素子を選択的にデータ線に接続する第１のスイッチ手段に、そのトランジスタのゲートを抵抗等により固定電位に接続するなどの電荷放電手段を付設することにより、水平アドレス線および垂直アドレス線の非選択時に第１のスイッチ手段に残存する電荷が放電され、水平アドレス線および垂直アドレス線の非選択切り替えの順序に関わらず確実に遮断される。

【００２３】また、読み出し手段が低入力インピーダンスおよび高出力インピーダンスを有するバッファまたは増幅器を有するものとしたときには、そのバッファまたは増幅器の出力を出力線に直接接続しても、出力線側から他の画素の出力が逆流することがない。

【００２４】請求項５のものでは、各画素の受光素子としてのフォトダイオードの両極が第１のトランジスタと第２のトランジスタに接続され、固定電位に接続する必要がないから、絶縁基板上に構成するのが容易である。

【００２５】

【発明の実施の形態】発明の実施の形態を実施例により説明する。図１は本発明の第１の実施例を示す図である。このイメージセンサは、垂直アドレス走査回路ＹＤに接続されたｍ本の垂直アドレス線Ｙ１～Ｙｍと水平アドレス走査回路ＸＤに接続されたｎ本の水平アドレス線Ｘ１～Ｘｎが格子状に配置され、ｎ本のデータ線ＤＬ１～ＤＬｎが水平アドレス線Ｘ１～Ｘｎと並んで配置されている。画素ＦＣ１は、受光素子であるフォトダイオー

ドDとフォトダイオードを選択的にデータ線に接続するスイッチ用のMOS型のトランジスタS1と垂直アドレス線に接続されるMOS型のトランジスタS2から構成される。

【0026】m×n個の画素FC1が2次元状に配置され、それぞれの画素FC1は、垂直アドレス線上の垂直アドレスyと水平アドレス線上の水平アドレスxにより制御される。説明を簡単にするために、図1には、m＝2、n＝2の場合のイメージセンサを示している。垂直アドレス線Y1と水平アドレス線X1に接続されている画素FC1を例にとり、その構成を説明する。MOS型のトランジスタS2のソースは水平アドレス線X1に、またゲートは垂直アドレス線Y1に接続されている。トランジスタS1のゲートはトランジスタS2に接続されている。

【0027】データ線DL1は、入力インピーダンス数百kΩのバッファB1の入力へ接続されている。バッファB1の出力は出力選択用のトランジスタQ1を介して出力線OLに接続される。トランジスタQ1のゲートは水平アドレス線X1に接続されている。出力線OLは出力バッファOBを介して出力端子Pに接続されている。同様にデータ線DL2もバッファB1とMOS型のトランジスタQ1を介して、出力線OLへ接続されている。

【0028】次に動作について説明する。入射光量に応じて光電変換された電荷はフォトダイオードDに蓄積される。まず、垂直アドレス線Y1と水平アドレス線X1が選択されると、トランジスタS2のゲートがハイになりターンオンする。トランジスタS2のソースもハイになっているので、トランジスタS1のゲートがハイになり、ターンオンされ、フォトダイオードDに蓄えられた電荷がデータ線DL1に分配される。この時には、出力選択用のトランジスタQ1も、ゲートが水平アドレス線X1に接続されているのでオンになっており、データ線DL1上の電荷はバッファB1およびトランジスタQ1を通り出力線OLに読み出される。

【0029】垂直アドレス線Y1と水平アドレス線X1のどちらか一方が選択されていなければ、トランジスタS1のゲートがハイになることはない。すなわち、MOSトランジスタS1は、水平アドレスx1と垂直アドレスy1を合わせた複合アドレス（x1・y1）により制御されている。

【0030】また、データ線DL2は入力インピーダンスが低いバッファB1に接続されているため、雑音電荷が取り込まれてもすぐにバッファB1の方へ流れ出すため、データ線DL2に雑音電荷が蓄積されることはない。さらに、データ線DL2はトランジスタQ1により出力線OLから分離されているため、出力線OLに接続される寄生容量はトランジスタQ1のみの小さなものとなる。また、バッファB1の出力インピーダンスを低くし、トランジスタQ1を近接させて配置することにより、バッファB1とトランジスタQ1の間をローインピーダンスに保ち、雑音電荷を拾うことを防止できる。

【0031】本実施例は以上のように構成され、フォトダイオードDをデータ線DL1、DL2、・・・に接続するトランジスタS1が、水平アドレスx1と垂直アドレスy1の複合アドレス（x1・y1）により制御されるため、ランダムアクセスが可能になる。また、データ線が入力インピーダンスの低いバッファB1に接続されているため、アクセスされていない列のデータ線はロー・インピーダンスに保たれ、スミアやシェーディングなどの偽信号の発生を防止できる。

【0032】さらに、バッファB1と出力線OLの間に出力選択用のトランジスタQ1が接続されているため、出力線OLの寄生容量が小さく、応答速度も速くなる。したがって、ランダムアクセスが可能で、また偽信号を防止でき、かつ応答速度も速いイメージセンサが得られる。

【0033】なお、本実施例では、データ線を垂直アドレス線と平行に配置しているが、これに限定されず、例えば図2に示すように、データ線DL′1およびDL′2を垂直アドレス線と平行に配置しバッファB′1と接続し、出力選択用のトランジスタQ′1を、垂直アドレス線により制御してもよく、また、データ線を斜めに配置したり、波状に配置することにより、設計上の自由度を向上させることができる。

【0034】次に本発明の第2の実施例について図3および図4を用いて説明する。図3は本実施例の構成を示す図である。図4は動作を説明するアドレス選択のタイミング図である。第1の実施例と同様に垂直アドレス線Y1と水平アドレス線X1に接続されている画素FC2を例にとり、その構成を説明する。画素FC2は、受光素子であるフォトダイオードDとフォトダイオードを選択的にデータ線に接続するスイッチ用のMOS型のトランジスタS3と、水平アドレス線X1とトランジスタS3のゲート間に配されたMOS型のトランジスタS4と、トランジスタS3のゲートに接続された抵抗R1から構成される。　トランジスタS4のゲートは垂直アドレス線Y1に接続されている。

【0035】データ線DL1は、入力インピーダンス数百kΩのバッファB1の入力へ接続されている。バッファB1の出力は加算器OAにより出力線OLに接続される。そして、出力線OLは出力バッファOBを介して出力端子Pに接続されている。同様に、データ線DL2も、バッファB1と加算器OAを介して出力線OLへ接続されている。

【0036】画素FC2の動作を説明するために、まず抵抗Rが接続されていないときの動作を説明する。画素FC2に抵抗R1が接続されていなければ、図1に示す実施例1と同様に、当該画素に接続されている水平アドレス線X1および垂直アドレス線Y1が選択されること

により、その画素のフォトダイオードDの電荷が出力線OLへ出力される。水平アドレス線X1と垂直アドレス線Y1は、特定の画素FC2を選択する場合には、どちらを先に選択しても動作に支障はない。しかし、選択状態から非選択状態に戻すときには、先に水平アドレス線X1が非選択状態になればトランジスタS3はターンオフし動作に支障はないが、もし垂直アドレス線Y1を先に非選択状態に戻すと、トランジスタS4がターンオフし、水平アドレス線X1とトランジスタS3のゲートが遮断されてしまう。

【0037】そのため、水平アドレス線X1を、その後に非選択にしても、トランジスタS3のゲート電荷が残ってしまい、トランジスタS3はターンオフできなくなってしまう。したがって、図4に示すように、まず水平アドレス線X（X1、X2、・・・）を非選択にしてから、垂直アドレス線Y（Y1、Y2、・・・）を非選択にしなければならない。

【0038】これに対して、抵抗R1を接続した場合には、抵抗R1がトランジスタS3の電荷の逃げ道になるため、先に垂直アドレス線Y1が非選択状態になりトランジスタS4がターンオフしても、トランジスタS3の電荷は抵抗R1を通って逃げることができるため、トランジスタS3はターンオフできる。　すなわち抵抗R1を接続すると、アドレス線を選択状態から非選択状態に戻すときの制御タイミングの制約がなくなる。抵抗R1は、トランジスタS3がP型のトランジスタの場合にはプルアップ回路を形成し、トランジスタS3がN型の場合にプルダウン回路となる。

【0039】加算器OAはバッファB1の出力を出力線OLに加算する。画素は垂直アドレスと水平アドレスにより、一つが選択されているため出力線OLには、選択された画素の情報のみが読み出される。なお、トランジスタS3のゲートの電位は、水平アドレスが選択された時の電位からトランジスタS4のしきい値を差し引いた電位なので、トランジスタS4がターンオンしても、トランジスタS3が十分にオンできないこともあるが、その場合には、あらかじめ、水平アドレスが選択された時の電位をブートストラップ等の方法で昇圧することにより、確実にトランジスタS3をターンオンすることができる。その他の構成および動作は図1に示す第1の実施例と同様である。

【0040】本実施例は以上のように構成され、まず、画素FC2に抵抗R1が加えられたことにより、トランジスタS3がターンオフしなくなることが防止され、アドレス線を選択状態から非選択状態に戻すときの制御タイミングの制約がなくなる。また、読み出し回路をバッファと加算器OAから構成することによりデータ線と出力線を分離しているため、水平アドレス線をバッファB1の出力まで延長する必要がなくなり、回路が簡素化される。したがって、第1の実施例と同様の効果が得られるとともに、制御タイミングの制約がなく、回路が簡略化されるという効果が得られる。

【0041】次に読み出し部の構成を変えた第3の実施例について説明する。　図5は全体の構成図を、図6は読み出し部の回路図を示す。本実施例では画素は第2の実施例のものと同構成である。読み出し部は、図6に詳細を示したバッファB2から構成される。バッファB2では、データ線DL1に数百kΩの抵抗R2の一端とMOSFET型のトランジスタT1のゲートが接続され、トランジスタT1のドレインがバッファB2の出力となっている。抵抗R2の他端は接地されている。トランジスタT1のソースも接地されており、トランジスタT1はソース接地型のトランジスタである。出力線OLには抵抗3が接続されている。

【0042】この実施例においては、画素FC2の電荷はデータ線DL1に読みだされ、読み出された電荷が、バッファB2においてデータ線DL1から抵抗R2を流れると電圧に変換される。変換された電圧をトランジスタT1のゲートに印加する。トランジスタT1を流れる電流は、そのゲート電圧、すなわち抵抗R2によって変換された電圧に比例する。データ線DL1を流れる電流に比例する電流が出力線OLを流れ、出力線OLに接続される抵抗R3により、電流が電圧に変換されて出力となる。

【0043】バッファB2では、データ線DL1に抵抗R2が接続されているので、データ線DL1がハイ・インピーダンスになることはなく、バッファB2の入力インピーダンスは低い。また、トランジスタT1はソース接地型のトランジスタであり、ドレインから見たトランジスタT1のインピーダンスは高く、数十MΩ以上になるので、バッファB2の出力インピーダンスは高くなる。

【0044】このため、直接バッファB2の出力を出力線OLに接続しても、出力線OL上で各バッファB2の出力が多入力OR接続となり、選択された画素FC2に接続されたデータ線を流れる電流に比例する電流が出力線OLを流れる。そして、他のバッファB2に漏れることがほとんど無く、出力線OLを流れる電流は電圧に変換されて出力となる。その他の構成および動作は図3に示す第2の実施例と同様である。

【0045】これにより第2実施例と同様の効果が得られるとともに、バッファB2のみで、データ線DLと出力線OLを接続することができるので、一層回路が簡素化される。なお、上記各実施例では、バッファを備えた読み出し部について説明したが、これに限定されず、増幅器を備えた読み出し部を用いることにより、読み出し感度を向上させることもできる。

【0046】次に、読み出し部の構成を変えた本発明の第4の実施例について説明する。図7は本実施例における読み出し部の回路図である。画素部は第2、第3の実

施例と同構成である。読み出し部はバッファＢ３から構成されている。バッファＢ３では、データ線ＤＬ１は数百ｋΩの抵抗Ｒ４の一端とＭＯＳＦＥＴ型のトランジスタＴ２のゲートに接続されている。抵抗Ｒ４の他端とトランジスタＴ２のソースは接地されている。トランジスタＴ２のドレインはＭＯＳＦＥＴ型のトランジスタＴ３のソースに接続されている。トランジスタＴ３のゲートは接地などの固定電位線ＦＬに接続されている。トランジスタＴ３のドレインはバッファＢ３の出力となり、出力線ＯＬに接続されている。出力線ＯＬにはダイオード接続されたＭＯＳＦＥＴ型のトランジスタＱ２が接続されている。

【００４７】この実施例では、バッファＢ３の抵抗Ｒ４とトランジスタＴ２により、データ線ＤＬ１を流れる電流に比例する電流が出力線ＯＬを流れ、出力線ＯＬに接続されるトランジスタＱ２により、電流が電圧に変換されて出力となる。バッファＢ３では、データ線ＤＬ１に抵抗Ｒ４が接続されているので、データ線ＤＬ１がハイ・インピーダンスになることはなく、バッファＢ３の入力インピーダンスは低い。また、トランジスタＴ２およびトランジスタＴ３はカスコード回路を構成し、トランジスタＴ３のドレインから見たインピーダンスはトランジスタＴ２のドレインから見たインピーダンスより大きくなっている。

【００４８】このため、バッファＢ３の出力インピーダンスが一層高くなり、直接バッファＢ３の出力を出力線ＯＬに接続しても、各バッファＢ３の出力が多入力ＯＲ接続となり、データ線ＤＬ１を流れる電流に比例する電流が出力線ＯＬを流れ、電圧に変換されて出力となる。また、カスコード接続によりバッファとしての応答速度も向上する。さらに、出力線ＯＬにダイオード接続されたトランジスタＱ２を抵抗の代わりに用いているので、増幅度も向上する。これにより第３の実施例と同様の効果が得られるとともに、バッファＢ３の出力インピーダンスが一層大きいので、出力線における電流電圧変換精度が向上し、また、応答速度が一層速くなる。

【００４９】図８は読み出し部の構成を変えた本発明の第５の実施例の読み出し部の回路図である。本実施例では読み出し部はバッファＢ４から構成されている。バッファＢ４では、データ線ＤＬ１は、ＭＯＳＦＥＴ型のトランジスタＴ４のゲートと接続されるとともに、ダイオード接続されたＭＯＳＦＥＴ型のトランジスタＴ５のゲートおよびドレインに接続されている。さらに、これらの接続点には電流源Ｉが接続されている。トランジスタＴ５のソースは固定電位に接続されている。トランジスタＴ４のソースは接地され、トランジスタＴ４のドレインがバッファＢ４の出力となり、出力線ＯＬに接続されている。画素部は、第１の実施例と同構成である。

【００５０】この実施例においては、バッファＢ４において、トランジスタＴ４とトランジスタＴ５がカレントミラー回路を構成し、電流源Ｉによりバイアスされている。データ線ＤＬ１を流れる電流はトランジスタＴ５を流れ、トランジスタＴ５を流れる電流に比例した電流がＴ４を流れるので、データ線ＤＬ１を流れる電流に比例した電流が出力線ＯＬを流れて、電圧に変換され出力される。バッファＢ４では、データ線ＤＬ１にトランジスタＴ５のドレインとゲートおよび電流源Ｉが接続されているので、データ線ＤＬ１がハイ・インピーダンスになることはなく、バッファＢ４の入力インピーダンスは低い。

【００５１】また、トランジスタＴ５およびトランジスタＴ４はカレントミラー回路を構成し、カレントミラー回路の出力インピーダンスは高く、バッファＢ４の出力を出力線ＯＬに直接接続しても、各バッファＢ４の出力が多入力ＯＲ接続となる。データ線ＤＬ１を流れる電流に比例する電流が出力線ＯＬを流れ、電圧に変換されて出力となる。その他の構成および動作は第４の実施例と同様であり、出力線ＯＬにはダイオード接続されたトランジスタＱ２が接続されている。

【００５２】これにより第３の実施例と同様の効果が得られるとともに、カレントミラー回路の使用により電流の取り出し精度が良くなるので、出力精度が向上する。、なお、本実施例では、カレントミラー回路を用いたが、これに限るものではなく、カスコード・カレントミラー回路や、ウィルソン型カレントミラー回路でも良く、また、カスコード回路を組み合わせれば、電流電圧変換精度や応答速度が向上する。

【００５３】図９は読み出し部の構成を変えた本発明の第６の実施例の読み出し部の回路図である。本実施例では読み出し部はバッファＢ５から構成されている。バッファＢ５では、データ線ＤＬ１はＭＯＳＦＥＴ型のトランジスタＴ６のソースに接続されている。トランジスタＴ６のゲートは固定電位線ＦＬに接続され、ドレインが出力線ＯＬに接続されている。出力線ＯＬには負荷用のＭＯＳＦＥＴ型のトランジスタＱ３が接続されている。その他の構成は、第１、第５の実施例と同じである。

【００５４】この実施例においては、トランジスタＴ６はゲート接地型トランジスタ回路であり、データ線ＤＬ１を流れる電流がトランジスタＴ６のソースとドレインを通って出力線に流れる。バッファＢ５では、トランジスタＴ６のソースから見たトランジスタＴ６のインピーダンスが低いため、データ線ＤＬ１がハイ・インピーダンスになることはなく、バッファＢ５の入力インピーダンスは低い。

【００５５】また、トランジスタＴ６のドレインから見たトランジスタＴ６のインピーダンスが高いため、バッファＢ５の出力を出力線ＯＬに直接接続しても、各バッファＢ５の出力が多入力ＯＲ接続となる。これにより、データ線ＤＬ１を流れる電流に比例する電流が出力線ＯＬを流れ、トランジスタＱ３により、電圧に変換されて

出力となる。さらに、ゲート接地回路はソース電流とドレイン電流が等しいため、電流取り出し精度が良いので、構成素子数も少なく、一つのトランジスタでよい。また、ミラー効果による信号の遅れもないため、応答速度も速い。これにより第3の実施例と同様の効果が得られるとともに、ゲート接地型トランジスタの使用により、出力精度が一層向上、回路が簡略化されかつ応答速度がより向上した。

【００５６】次に画素の構成を変えた本発明の第７の実施例について説明する。図１０は本実施例の画素の回路図である。画素ＦＣ３は、受光素子であるフォトダイオードＤとフォトダイオードを選択的にデータ線に接続するスイッチ用のＭＯＳトランジスタＳ５と垂直アドレス線に接続されるＭＯＳトランジスタＳ６とフレーム転送用のスイッチであるＳ７とフォトダイオードのリセット用のスイッチであるトランジスタＳ８から構成される。

【００５７】ＭＯＳトランジスタＳ６のソースは水平アドレス線Ｘ１に、そのゲートは垂直アドレス線Ｙ１にそれぞれ接続されている。トランジスタＳ５のゲートはＭＯＳトランジスタＳ６のドレインに接続されている。トランジスタＳ７はフォトダイオードＤとトランジスタＳ８に接続されている。トランジスタＳ７のゲートにはフレームシフト信号ＦＳが入力され、トランジスタＳ８のゲートにはリセット信号ＲＳが入力される。また、トランジスタＳ８の残りの電極はリセット電位に接続されている。

【００５８】この実施例では、トランジスタＳ６により複合アドレスが生成され、トランジスタＳ５によりフォトダイオードＤとデータ線ＤＬ１が接続される。また、トランジスタＳ７のゲートにフレームシフト信号ＦＳが入力されると、各画素ＦＣ３の電荷が転送される。さらに、トランジスタＳ８にリセット信号ＲＳが入力されると、フォトダイオードＤのアノードがリセット電位に接続され、フォトダイオードＤはリセットされる。なお、読み出し部の構成は、図９の第６の実施例におけると同じである。

【００５９】これにより、第１の実施例と同様の効果が得られるとともに、フレーム転送が可能になる。また、フォトダイオードＤのリセットが可能になり、電子シャッターを実現することができ、一層実用上の利便性が向上する。なお、上記各実施例では、フォトダイオードＤのカソードが固定電位に接続されているが、これに限定されず、アノードが固定電位に接続されてもよく、フォトダイオードＤのどちらかの電極が固定電位に接続されればよい。

【００６０】図１１は画素の構成を変えた本発明の第８の実施例の画素の回路図である。本実施例の画素ＦＣ４では、受光素子であるフォトダイオードＤのアノードがスイッチ用のＭＯＳ型トランジスタＳ９を介してデータ線ＤＬ１に接続され、カソードはＭＯＳ型トランジスタＳ１０を介して固定電位に接続されている。トランジスタＳ９のゲートは垂直アドレス線Ｙ１に、トランジスタＳ１０のゲートは水平アドレス線Ｘ１に接続されている。

【００６１】本実施例では基板にＳＯＩ等の絶縁基板を使用する場合にも、フォトダイオードＤを固定電位に接続する必要なしに、トランジスタＳ９とトランジスタＳ１０のそれぞれが、複合アドレスの生成とデータ線接続の選択動作の両方の機能を同時に果たし、水平・垂直アドレス線が同時に選択された画素の光電荷がデータ線ＤＬ１に送出される。読み出し部は、第６、第７の実施例と同構成である。

【００６２】これにより、第１の実施例と同様の効果が得られるとともに、フォトダイオードＤを固定電位に接続する必要が無いので、設計上の自由度が向上し、画像処理等の画素として使用する際には、画素を微細化でき、画像の分解能を向上させることができる。なお、第７、第８の実施例では読み出し部の構成を第６の実施例と同じもので説明したが、その他第１から第５の各実施例における読み出し部の構成と任意に組み合わせることにより、各実施例毎に説明した追加の効果を得ることができる。

【００６３】

【発明の効果】以上のとおり、本発明は、受光素子をデータ線に接続するスイッチ手段が、水平アドレスと垂直アドレスの複合アドレスにより制御されるため、ランダムアクセスが可能になる。また、データ線が低入力インピーダンスを有する読み出し手段を介して出力線に接続されているので、データ線がロー・インピーダンスに保たれ、出力線の寄生容量が増大しないから、スミアやシェーディングも防止される。

【００６４】なお、受光素子を選択的にデータ線に接続する第１のスイッチ手段に電荷放電手段を付設することにより、水平アドレス線および垂直アドレス線の非選択時に第１のスイッチ手段に残存する電荷が放電され、水平アドレス線および垂直アドレス線の非選択切り替えの順序に関わらず確実に遮断されるという効果が得られる。

【００６５】また、読み出し手段がバッファまたは増幅器と出力線の間に出力選択手段または加算手段を備えることにより、出力線の寄生容量が小さくなり、応答速度も速くなる。さらに、読み出し手段が低入力インピーダンスおよび高出力インピーダンスを有するバッファまたは増幅器を有するものとしたときには、そのバッファまたは増幅器の出力を出力線に直接接続することができ、回路が簡素化されたイメージセンサが得られる。

【図面の簡単な説明】

【図１】本発明の第１の実施例を示す図である。

【図２】データ線配置の変形例を示す図である。

【図３】第２の実施例を示す図である。

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【図4】アドレス選択タイミングの説明図である。
【図5】第3の実施例を示す図である。
【図6】第3の実施例の読み出し部の回路図である。
【図7】第4の実施例を示す図である。
【図8】第5の実施例を示す図である。
【図9】第6の実施例を示す図である。
【図10】第7の実施例を示す図である。
【図11】第8の実施例を示す図である。
【図12】従来例を示す図である。
【図13】従来例における問題を説明する図である。
【図14】複合アドレスの説明図である。
【符号の説明】
B1、B′1、B2、B3、B4、B5　バッファ
D　フォトダイオード（受光素子）
DL1、DL2、DL′1、DL′2　データ線
FC1、FC2、FC3、FC4、FC5　画素
H　光源
I　電流源
OA　加算器（加算手段）
OB　出力バッファ
OL　出力線

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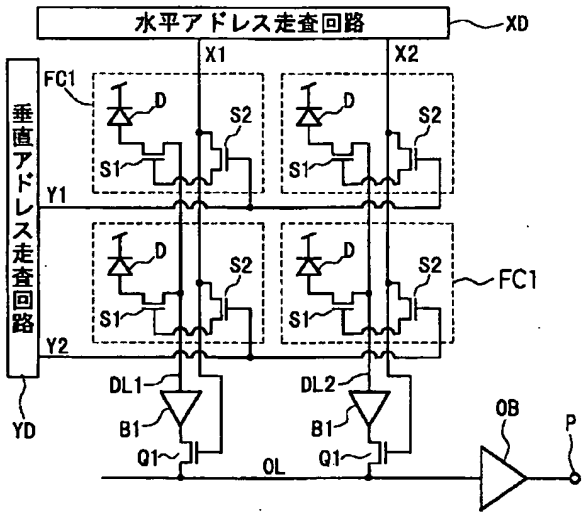
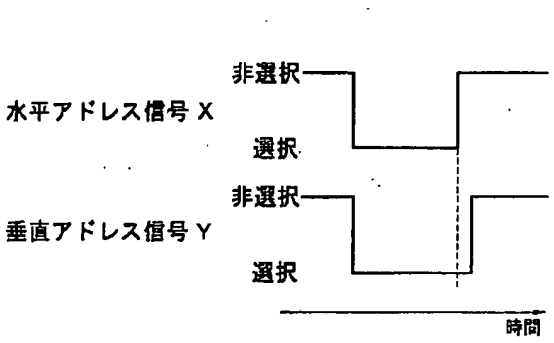
P　出力端子
Q1、Q′1　トランジスタ（出力選択手段）
Q2、Q3、Q4　トランジスタ
R1　抵抗（電荷放電手段）
R2、R3、R4　抵抗
S1、S3、S5　トランジスタ（第1のスイッチ手段）
S2、S4、S6　トランジスタ（第2のスイッチ手段）
S7、S8　トランジスタ
S9　トランジスタ（第1のトランジスタ）
S10　トランジスタ（第2のトランジスタ）
S12　トランジスタ（スイッチ手段）
SU　スミア
T1、T2、T3、T4、T5、T6　トランジスタ
X1、X2　水平アドレス線
XD　水平アドレス走査回路
Y1、Y2　垂直アドレス線
YD　垂直アドレス走査回路

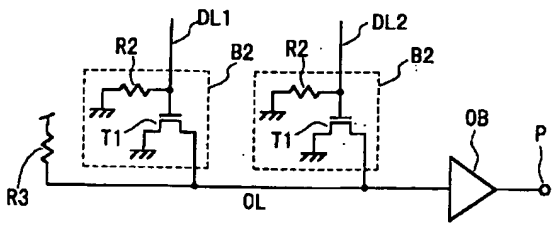
【図1】



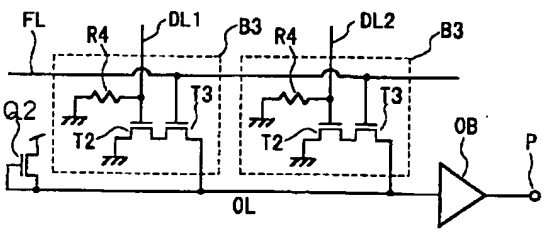
【図4】



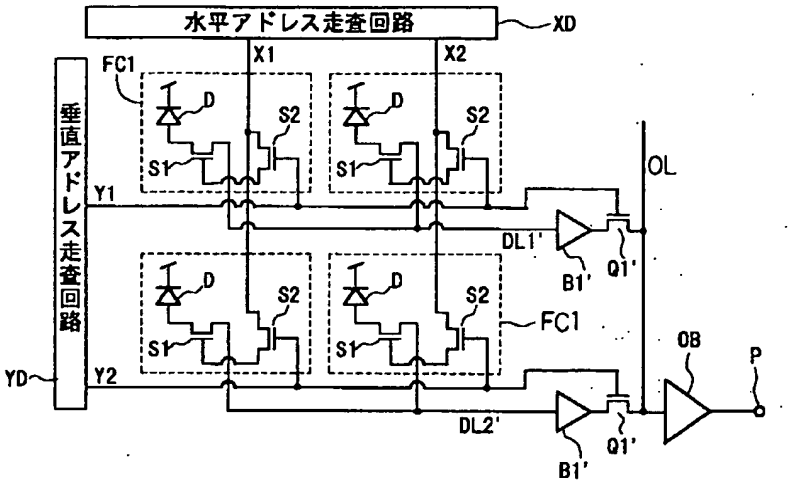
【図6】



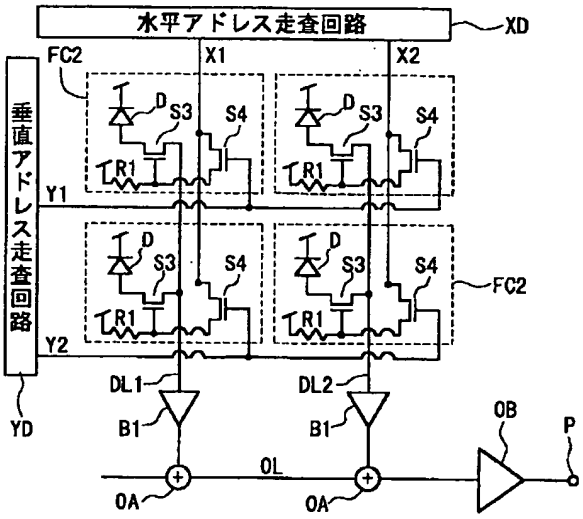
【図7】



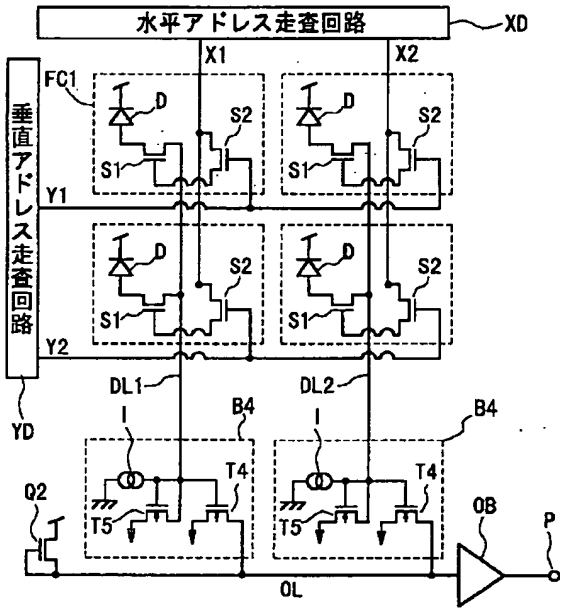
【図2】


水平アドレス走査回路
XD
X1
X2
FC1
D
S1
S2
垂直アドレス走査回路
Y1
Y2
YD
OL
DL1'
DL2'
B1'
Q1'
OB
P

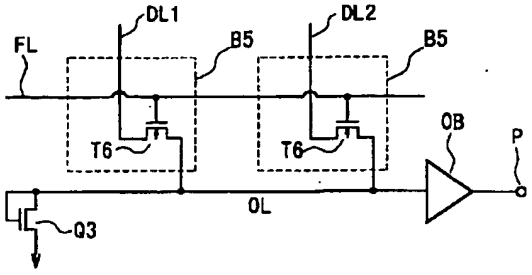
【図3】


水平アドレス走査回路
XD
X1
X2
FC2
D
S3
S4
R1
垂直アドレス走査回路
Y1
Y2
YD
DL1
DL2
B1
OL
OA
OB
P

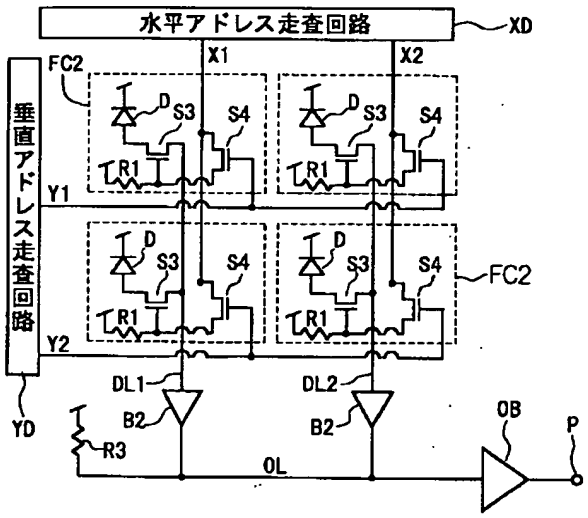
【図8】


水平アドレス走査回路
XD
X1
X2
FC1
D
S1
S2
垂直アドレス走査回路
Y1
Y2
YD
DL1
DL2
B4
T4
T5
Q2
OL
OB
P

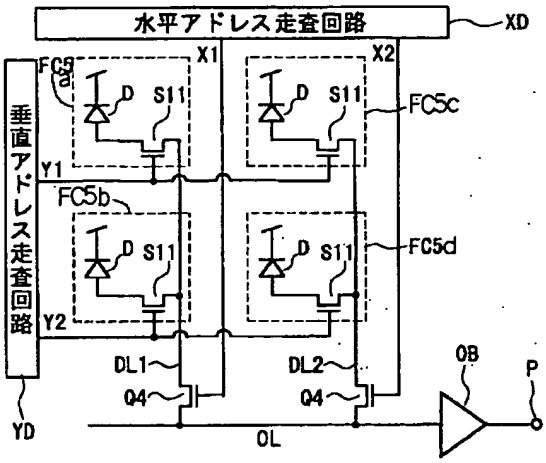
【図9】


FL
DL1
DL2
B5
T6
OL
Q3
OB
P

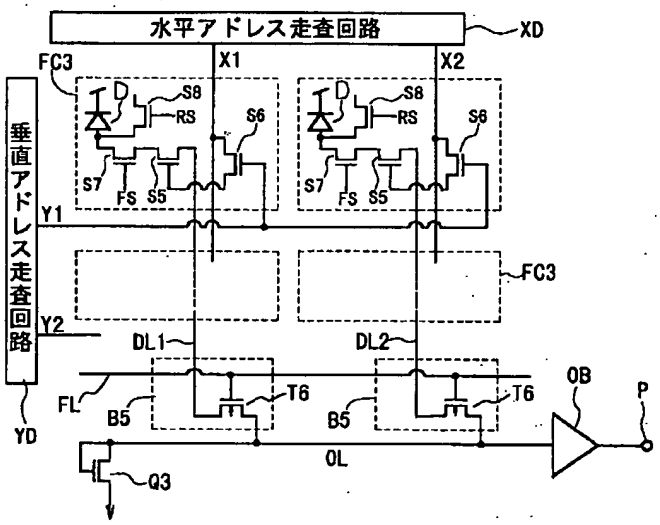
【図5】



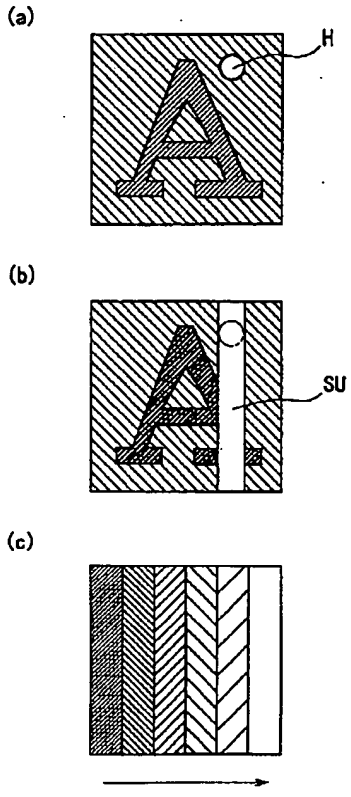
【図12】



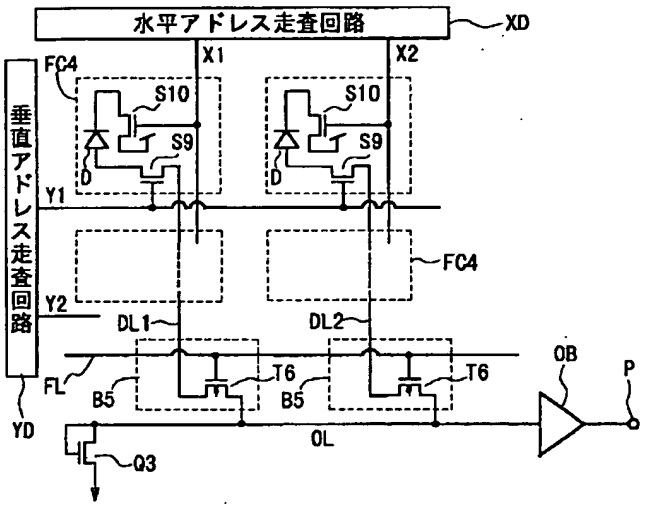
【図10】



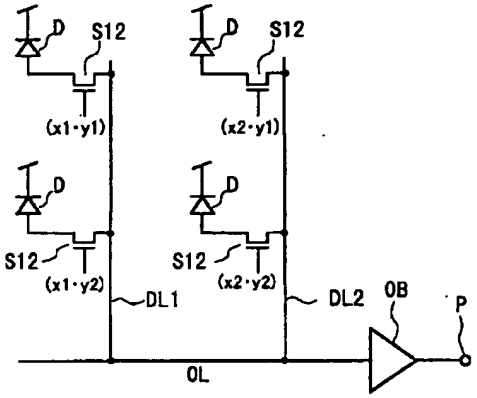
【図13】



【図11】


水平アドレス走査回路
XD
X1
X2
FC4
S10
S9
D
Y1
Y2
垂直アドレス走査回路
DL1
DL2
FL
B5
T6
OB
P
YD
OL
Q3

【図14】


D
S12
(x1・y1)
(x2・y1)
(x1・y2)
(x2・y2)
DL1
DL2
OB
P
OL